



# SGM811B/SGM812B Microprocessor Supervisory Circuits with Manual Reset Input

## GENERAL DESCRIPTION

The SGM811B/SGM812B supervisory circuits monitor the power supply voltage in microprocessor and digital systems. The SGM811B/SGM812B are designed to monitor three different voltages, these voltages have been selected for the effective monitoring of 3V and 3.3V supply voltage levels.

They provide a reset output during power-up, power-down and brownout conditions. On power-up, an internal timer holds reset asserted for 200ms. This holds the microprocessor in a reset state until conditions have stabilized. The nRESET output remains operational with  $V_{CC}$  as low as 1V. The SGM811B provides an active low reset signal (nRESET) while the SGM812B provides an active high signal (RESET) output.

Included in this circuit is a manual reset input. The manual reset function is very useful, especially if the circuit in which the SGM811B/SGM812B is operating enters into a state that can only be detected by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out-of-control or locked system. The devices come in SOT-143 package.

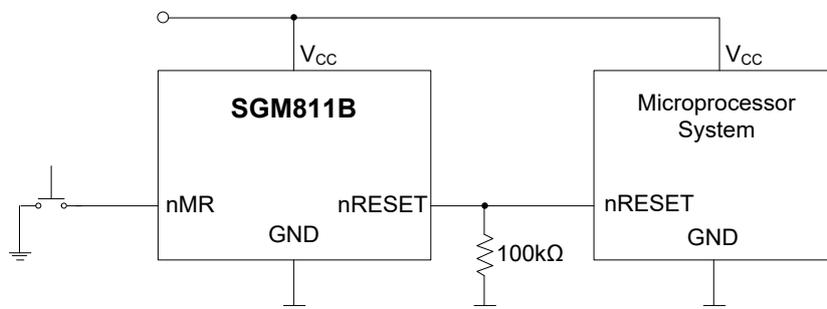
## FEATURES

- Superior Upgrade for MAX811/MAX812 and ADM811/ADM812
- Fully Specified over Temperature
- Low Power Consumption < 1 $\mu$ A (TYP)
- Precision Voltage Monitor: 3V and 3.3V Options
- Reset Assertion Down to 1V  $V_{CC}$
- 200ms Power-On Reset (TYP)
  - Logic Low nRESET Output (SGM811B)
  - Logic High RESET Output (SGM812B)
- Manual Reset Input
- -40°C to +125°C Operating Temperature Range
- Available in Green SOT-143 Package

## APPLICATIONS

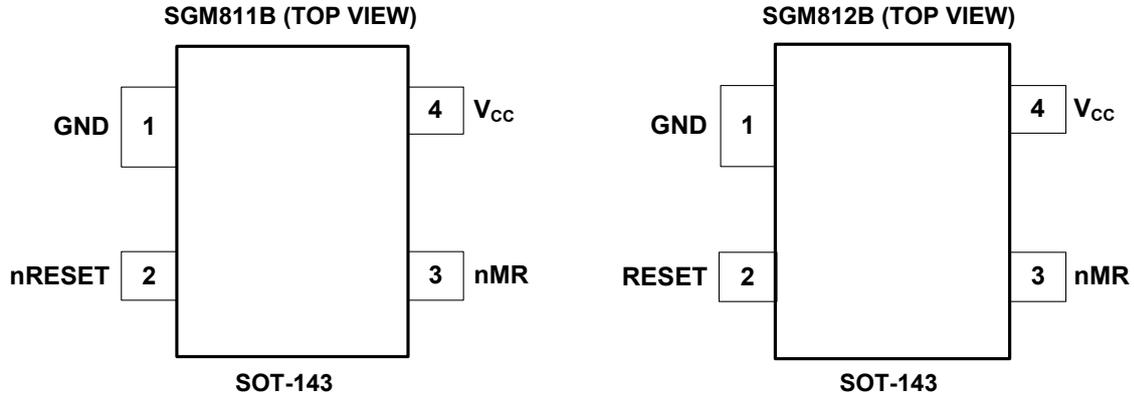
Microprocessor Systems  
Controllers  
Intelligent Instruments  
Automotive Systems  
Safety Systems  
Portable Instruments

## TYPICAL APPLICATION





**PIN CONFIGURATION**



**PIN DESCRIPTION**

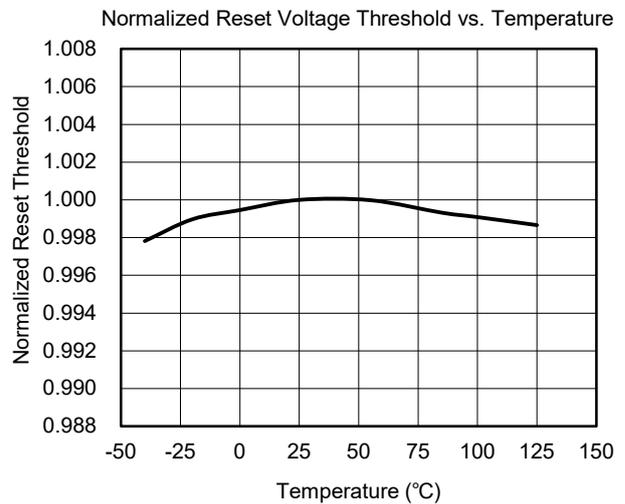
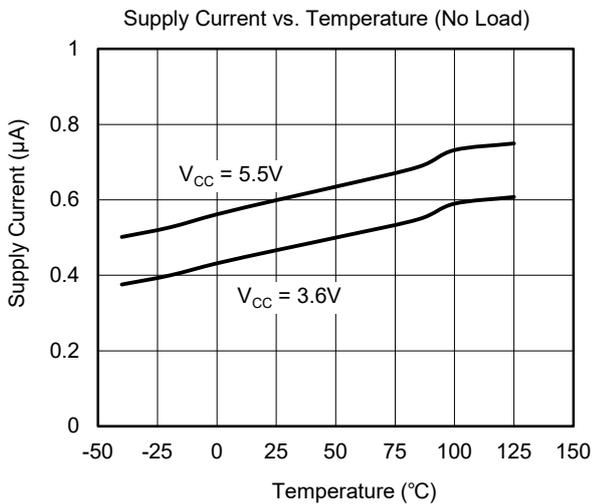
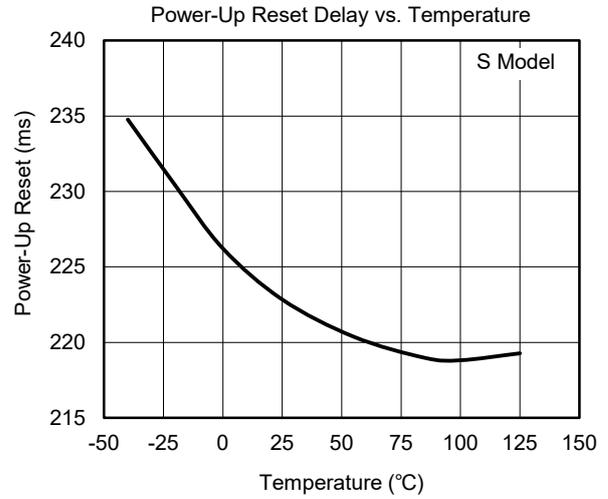
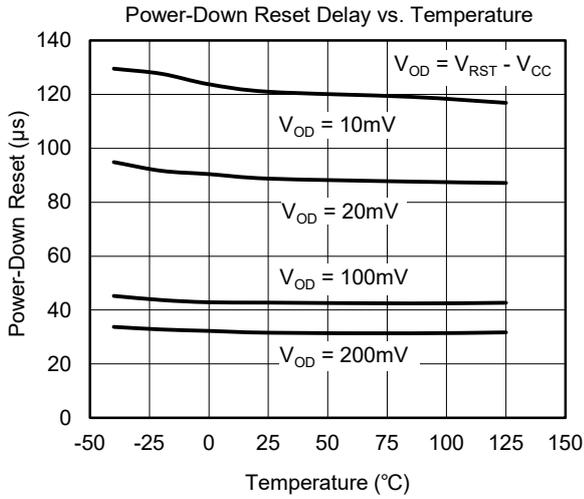
NAME	PIN NUMBER		FUNCTION
	SGM811B	SGM812B	
GND	1	1	Ground.
nRESET	2	—	Active Low Logic Output. nRESET remains low while V <sub>CC</sub> is below the reset threshold or when nMR is low; nRESET then remains low for 200ms (TYP) after V <sub>CC</sub> rises above the reset threshold.
RESET	—	2	Active High Logic Output. RESET remains high while V <sub>CC</sub> is below the reset threshold or when nMR is low; RESET then remains high for 200ms (TYP) after V <sub>CC</sub> rises above the reset threshold.
nMR	3	3	Manual Reset Input Pin. A logic low on nMR asserts reset. Reset remains asserted as long as nMR is held low and for 200ms after nMR returns high. The active-low input has an internal 59kΩ pull-up resistor. It can be driven from a CMOS logic line or shorted to ground with a switch. Leave open or connect to V <sub>CC</sub> if unused.
V <sub>CC</sub>	4	4	Power Supply Voltage. Power supply voltage that is monitored.

**ELECTRICAL CHARACTERISTICS**

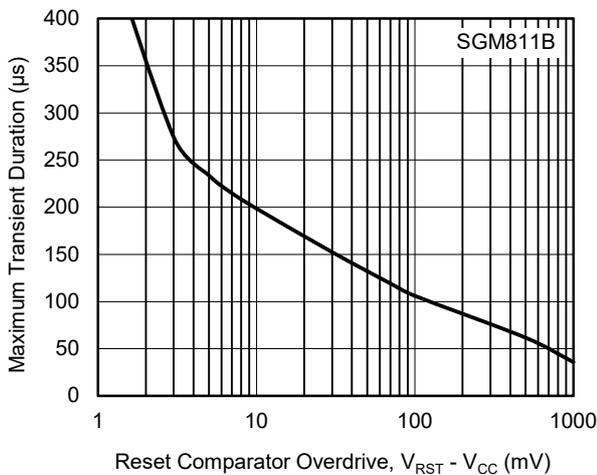
(T<sub>A</sub> = +25°C, V<sub>CC</sub> = 3.3V for T/S Models, V<sub>CC</sub> = 3V for R Model, Full = -40°C to +125°C, unless otherwise noted.)

PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Operating Voltage Range (V <sub>CC</sub> )		Full	1.0		5.5	V
Supply Current (I <sub>SUPPLY</sub> )	V <sub>CC</sub> = 3.6V	Full		0.5	1.0	μA
	V <sub>CC</sub> = 5.5V	Full		0.6	1.4	
Reset Threshold (V <sub>RST</sub> )	T Model	+25°C	3.03	3.08	3.14	V
		Full	3.03		3.15	
	S Model	+25°C	2.88	2.93	2.98	
		Full	2.87		2.99	
	R Model	+25°C	2.59	2.63	2.67	
		Full	2.58		2.68	
Reset Threshold Hysteresis	T Model	+25°C		13		mV
	S Model	+25°C		13		
	R Model	+25°C		12		
Reset Threshold Temperature Coefficient		Full		20		ppm/°C
V <sub>CC</sub> to Reset Delay (t <sub>RD</sub> )	V <sub>RST</sub> - V <sub>CC</sub> = 100mV	+25°C		100		μs
Reset Pulse Width (t <sub>RS</sub> )		Full	140	200	290	ms
<b>MANUAL RESET</b>						
Minimum Pulse Width		Full	300			ns
Glitch Immunity		+25°C		130		ns
Reset Propagation Delay		Full			400	ns
Pull-Up Resistance		Full	40	59	81	kΩ
The Manual Reset Circuit Will Act On:						
An Input Rising Above	V <sub>CC</sub> > V <sub>RST(MAX)</sub>	Full	0.7 × V <sub>CC</sub>			V
An Input Falling Below	V <sub>CC</sub> > V <sub>RST(MAX)</sub>	Full			0.3 × V <sub>CC</sub>	
<b>nRESET/RESET OUTPUT VOLTAGE</b>						
Low (SGM811B)	V <sub>CC</sub> = V <sub>RST(MIN)</sub> , I <sub>SINK</sub> = 1.2mA	Full			0.4	V
Low (SGM811B)	V <sub>CC</sub> > 1.0V, I <sub>SINK</sub> = 50μA	Full			0.3	
High (SGM811B)	V <sub>CC</sub> > V <sub>RST(MAX)</sub> , I <sub>SOURCE</sub> = 500μA	Full	0.8 × V <sub>CC</sub>			
Low (SGM812B)	V <sub>CC</sub> = V <sub>RST(MAX)</sub> , I <sub>SINK</sub> = 1.2mA	Full			0.4	
High (SGM812B)	1.8V < V <sub>CC</sub> < V <sub>RST(MIN)</sub> , I <sub>SOURCE</sub> = 150μA	Full	0.8 × V <sub>CC</sub>			

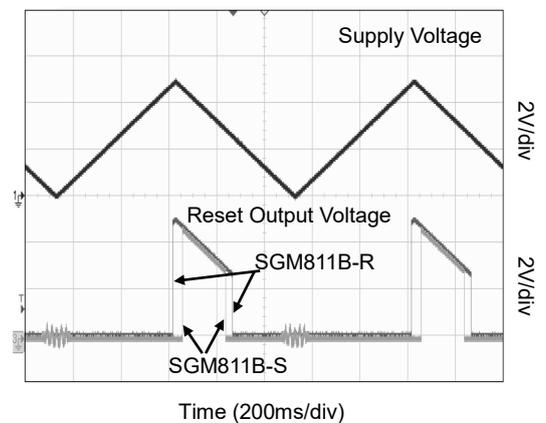
**TYPICAL PERFORMANCE CHARACTERISTICS**



Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive



Reset Output Voltage vs. Supply Voltage



**APPLICATION INFORMATION**

**Manual Reset**

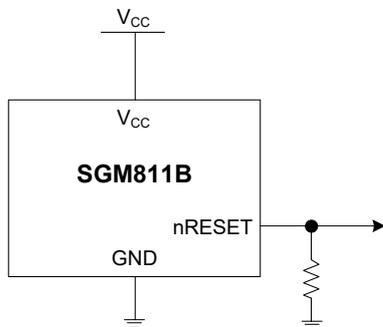
Many  $\mu$ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the SGM811B/SGM812B, a logic low on nMR asserts reset. Reset remains asserted while nMR is low, and for  $t_{RS}$  (200ms nominal) after it returns high. nMR has an internal 59k $\Omega$  pull-up resistor, so it can be left open if not used. This input can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from nMR to GND to create a manual reset function; external debounce circuitry is not required. If nMR is driven from long cables or the device is used in a noisy environment, connect a 0.1 $\mu$ F capacitor from nMR to GND to provide additional noise immunity.

**Very Accurate Reset Threshold**

Because the SGM811B/SGM812B can operate effectively even when there are large degradations of the supply voltages, the possibility of a malfunction during a power failure is greatly reduced. Another advantage of the SGM811B/SGM812B is its very accurate internal voltage reference circuit. Combined, these benefits produce an exceptionally reliable microprocessor supervisory circuit.

**Ensuring a Valid Reset Output Down to  $V_{CC} = 0V$**

When  $V_{CC}$  falls below 1.0V, the SGM811B's nRESET no longer sinks current. Therefore, a high impedance CMOS logic input connected to nRESET may drift to undetermined logic levels. To eliminate this problem, a 100k $\Omega$  resistor should be connected from nRESET to ground.



**Figure 1. Ensuring a Valid nRESET Output Down to  $V_{CC} = 0V$**

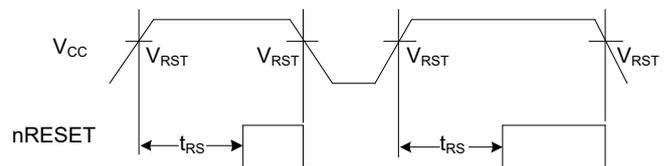
**Reset Output**

On power-up and after  $V_{CC}$  rises above the reset threshold, an internal timer holds the reset output active for 200ms (TYP). This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 200ms (TYP) after the supply recovers. This allows time for the power supply and microprocessor to stabilize.

The SGM811B provides an active low reset output (nRESET) while the SGM812B provides an active high output (RESET). During power-down of the SGM811B, the nRESET output remains valid (low) with  $V_{CC}$  as low as 1V. This ensures that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures that no spurious activity can occur via the microprocessor as it powers up.

**Glitch Immunity**

The SGM811B/SGM812B contain internal filtering circuitry providing glitch immunity from fast transient glitches on the power supply line.



**Figure 2. Power Fail nRESET Timing**

**Interfacing to Other Devices Output**

The SGM811B/SGM812B are designed to integrate with as many devices as possible. One feature of the SGM811B/SGM812B is the reset output, which is directly proportional to  $V_{CC}$  (this is guaranteed only while  $V_{CC}$  is greater than 1V). This enables the part to be used with both 3V and 3.3V, or any nominal voltage within the minimum and maximum specifications for  $V_{CC}$ .

**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Original (DECEMBER 2018) to REV.A**

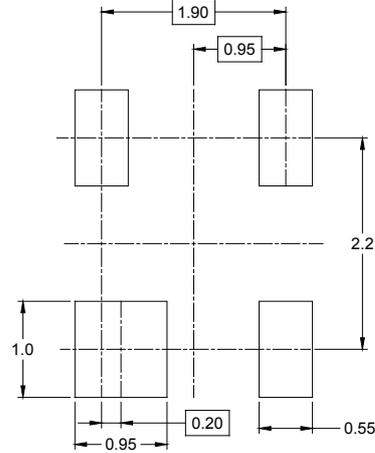
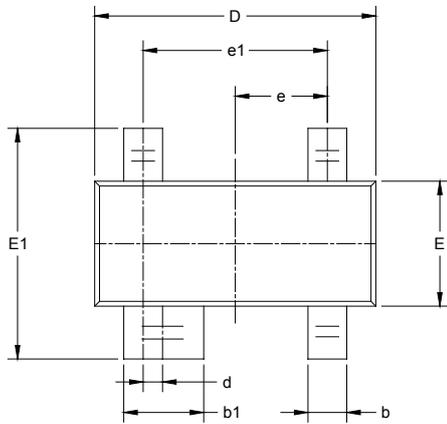
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Changed from product preview to production data.....All

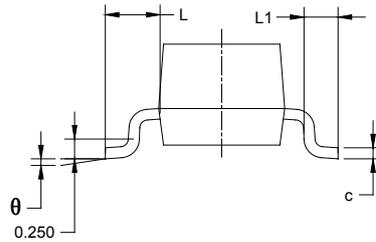
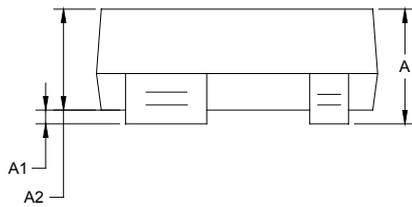
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PACKAGE OUTLINE DIMENSIONS

SOT-143



RECOMMENDED LAND PATTERN (Unit: mm)

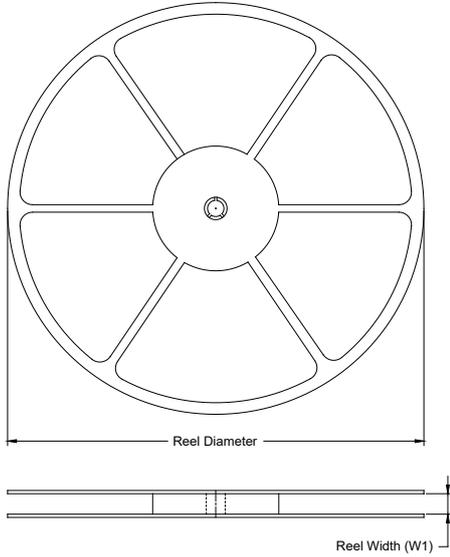


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
b1	0.750	0.900	0.030	0.035
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
d	0.200 TYP		0.008 TYP	
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.55 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
$\theta$	0°	8°	0°	8°

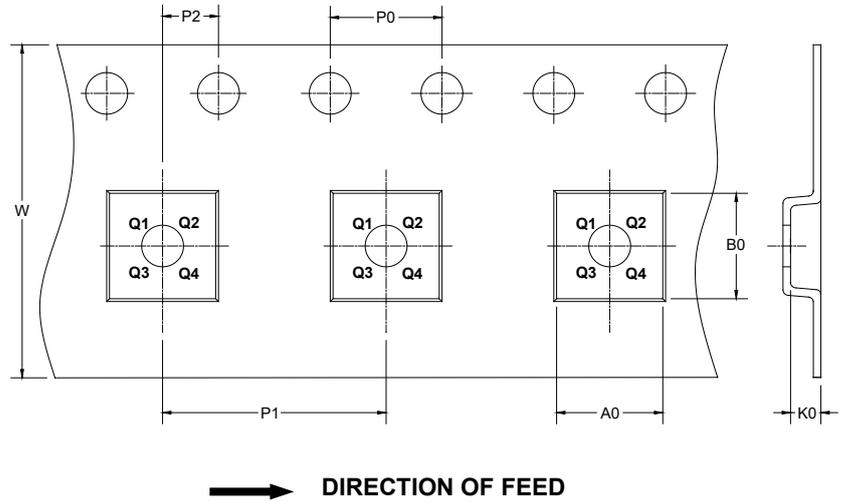
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

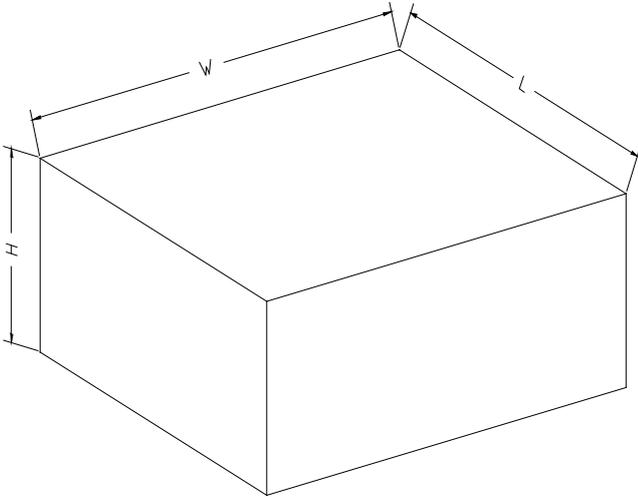
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-143	7"	9.5	3.20	2.80	1.30	4.0	4.0	2.0	8.0	Q3

000001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002