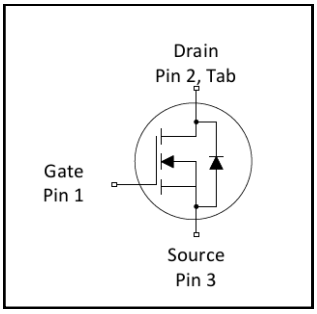
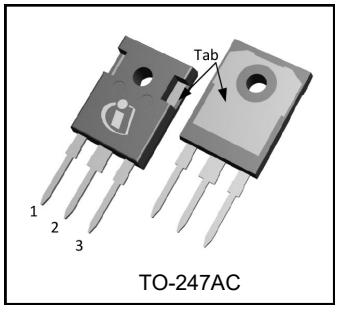
IRFP3077PbF

V_{DSS}	75V
$R_{DS(on)}$ typ.	2.8mΩ
max.	3.3mΩ
$I_{D\ (Silicon\ Limited)}$	200A①
$I_{D\ (Package\ Limited)}$	120A





TO-247AC

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Worldwide Best RDS(on) in TO-247
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP3077PbF	TO-247	Tube	25	IRFP3077PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	200①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V(Silicon Limited)	140①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ②	850	
P_D @T_C = 25°C	Maximum Power Dissipation	340	W
	Linear Derating Factor	2.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	2.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	200	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.44	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient⑧	—	40	

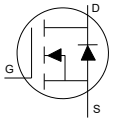
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.091	—	V/°C	Reference to 25°C, I_D = 5mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.8	3.3	mΩ	V_{GS} = 10V, I_D = 75A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 75V, V_{GS} = 0V
		—	—	250		V_{DS} = 75V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	—	1.2	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specfied)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	160	—	—	S	V_{DS} = 50V, I_D = 75A
Q_g	Total Gate Charge	—	160	220	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge	—	37	—		V_{DS} =38V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	42	—		V_{GS} = 10V ⑤
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	V_{DD} = 38V
t_r	Rise Time	—	87	—		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	—	69	—		R_G = 2.1Ω
t_f	Fall Time	—	95	—		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	—	9400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	820	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	350	—		f = 1.0 MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ⑦	—	1090	—		V_{GS} = 0V, V_{DS} = 0V to 60V ⑦See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related) ⑥	—	1260	—		V_{GS} = 0V, V_{DS} = 0V to 60V ⑥See Fig. 5

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	200①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	850		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	42	63	ns	T_J = 25°C
		—	50	75		T_J = 125°C
Q_{rr}	Reverse Recovery Charge	—	59	89	nC	T_J = 25°C
		—	86	130		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	2.5	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by				

V_R = 64V, I_F = 75A di/dt = 100A/µs ⑤

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A.Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. Junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.028mH, R_G = 50Ω, I_{AS} = 120A,V_{GS} =10V. Part not Recommended for use above this value.

④ ISD ≤ 75A, di/dt ≤ 400A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

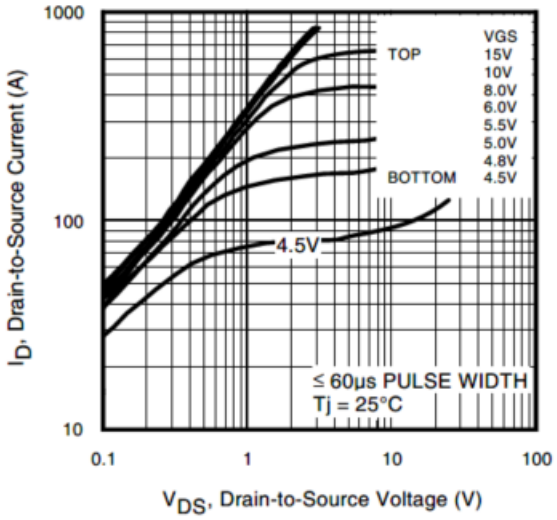


Fig 1. Typical Output Characteristics

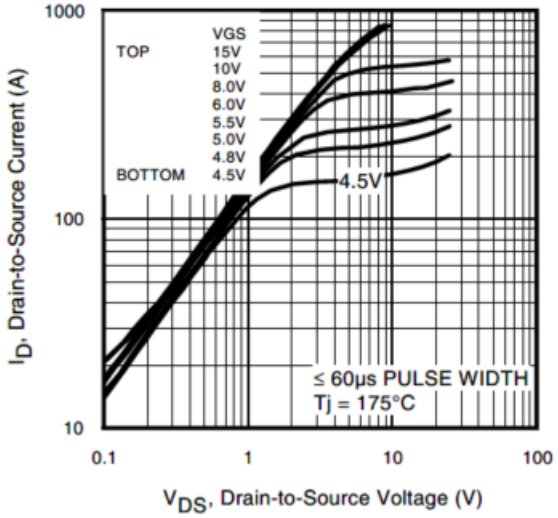


Fig 2. Typical Output Characteristics

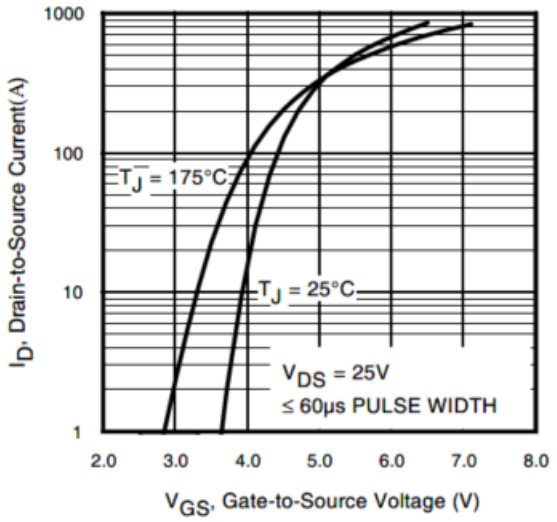


Fig 3. Typical Transfer Characteristics

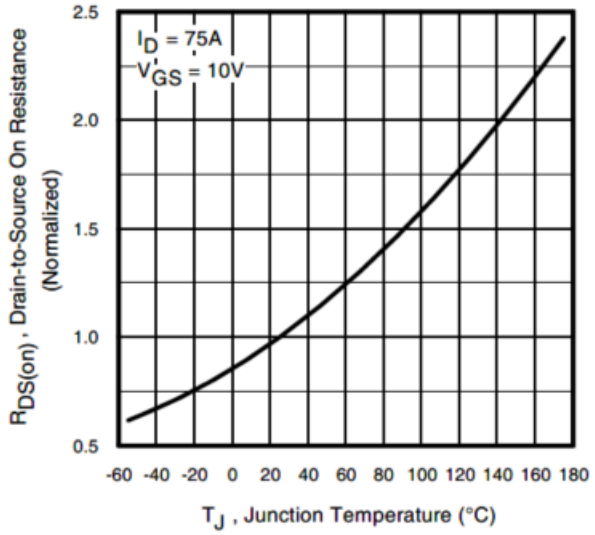


Fig 4. Normalized On-Resistance vs. Temperature

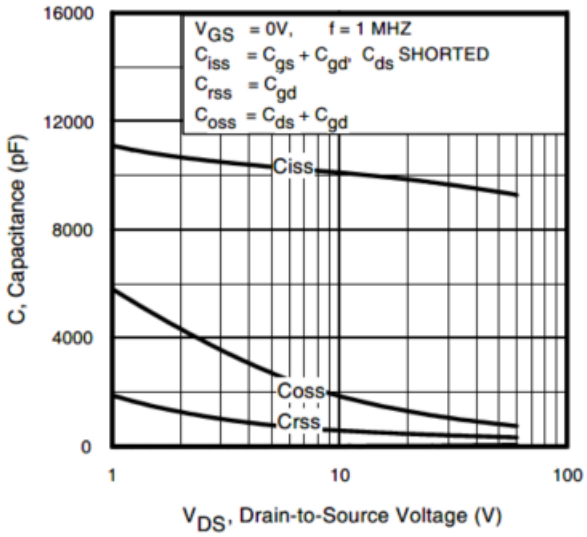


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

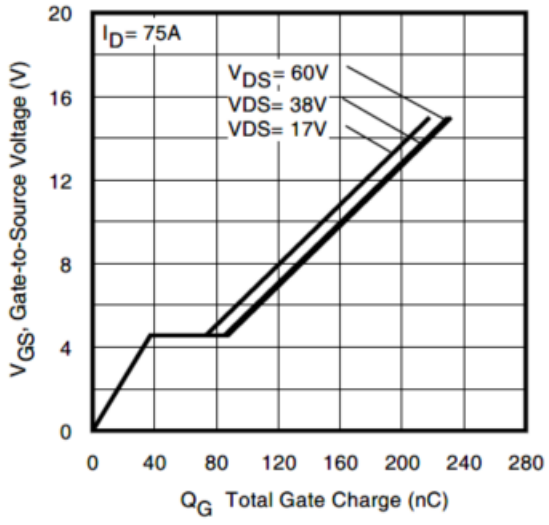


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

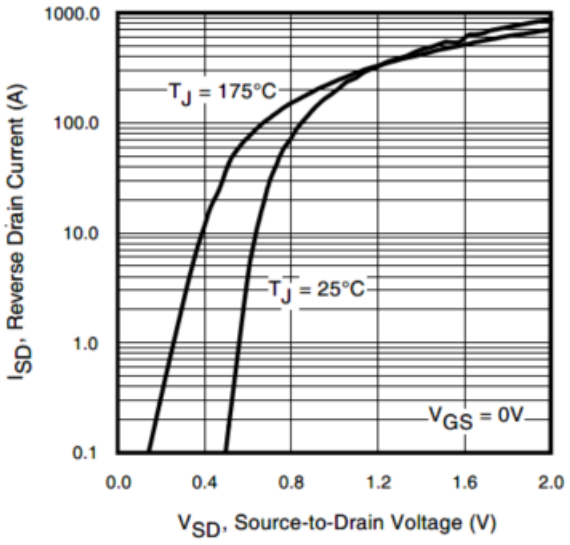


Fig 7. Typical Source-to-Drain Diode Forward Voltage

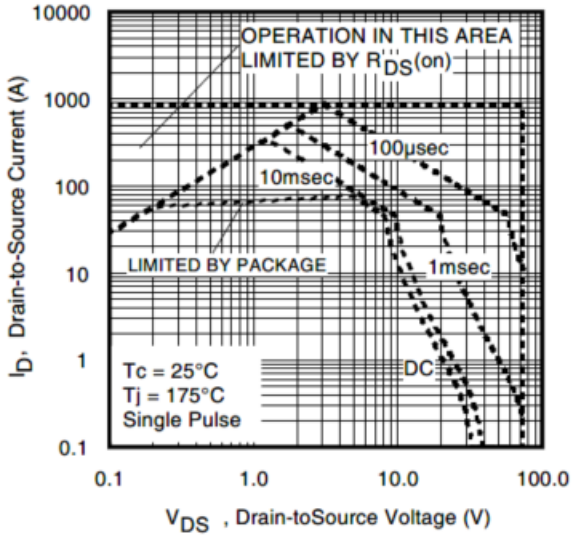


Fig 8. Maximum Safe Operating Area

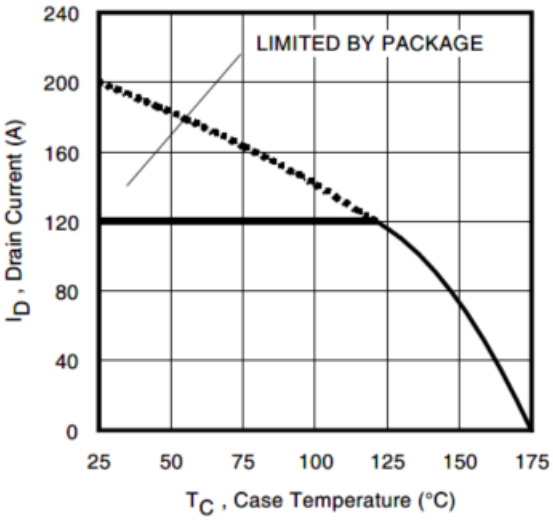


Fig 9. Maximum Drain Current vs. Case Temperature

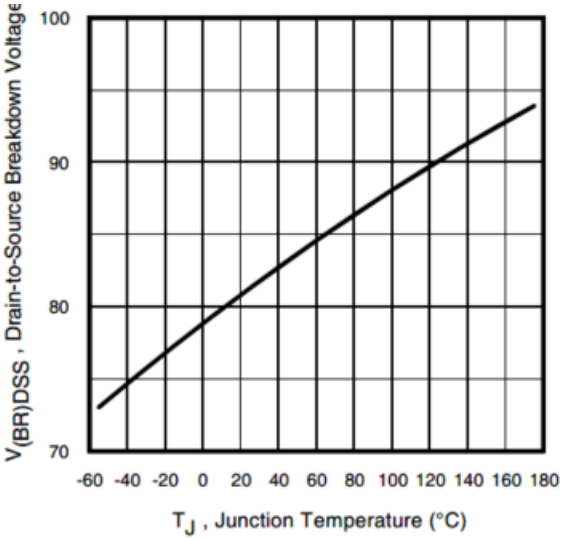


Fig 10. Drain-to-Source Breakdown Voltage

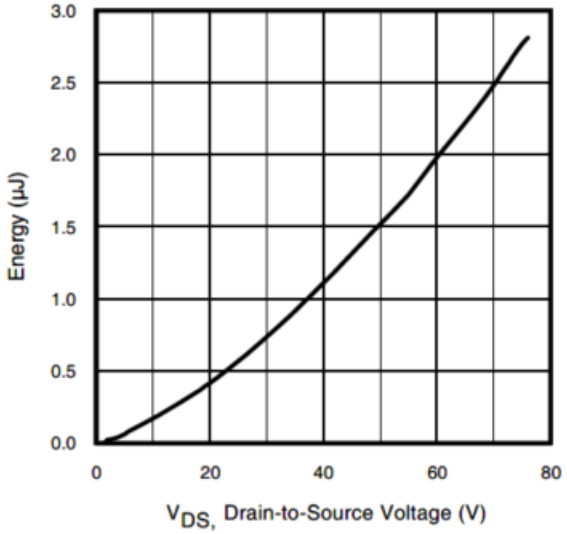


Fig 11. Typical Coss Stored Energy

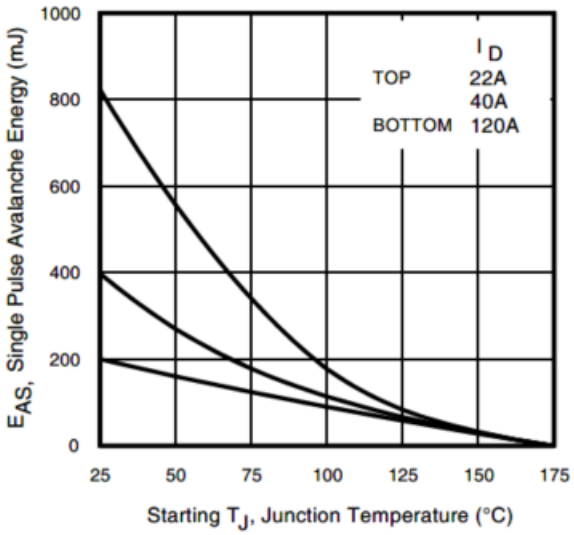


Fig 12. Maximum Avalanche Energy vs. Drain Current

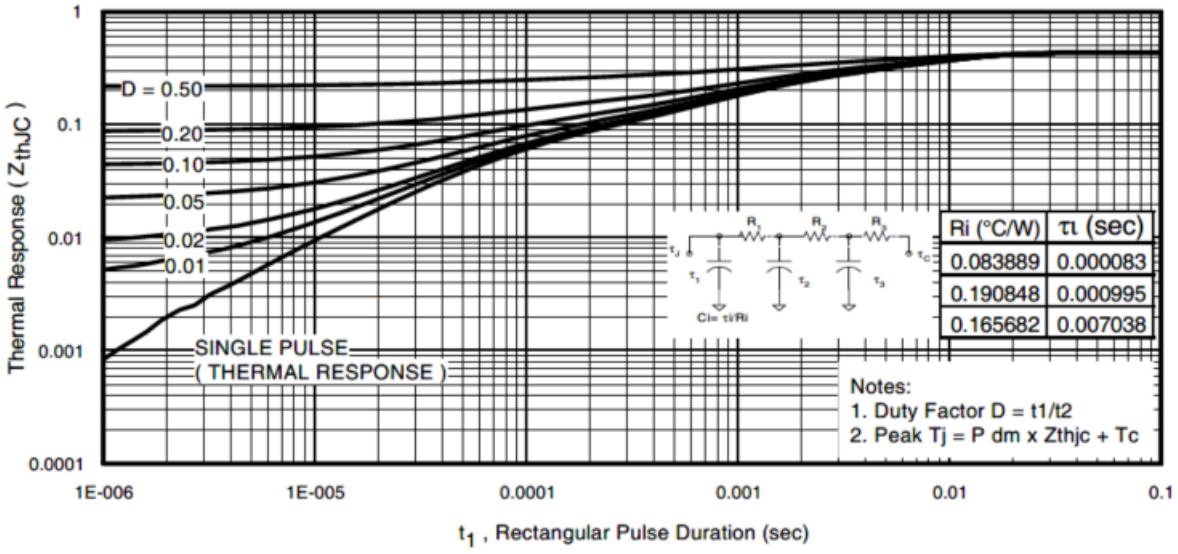


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

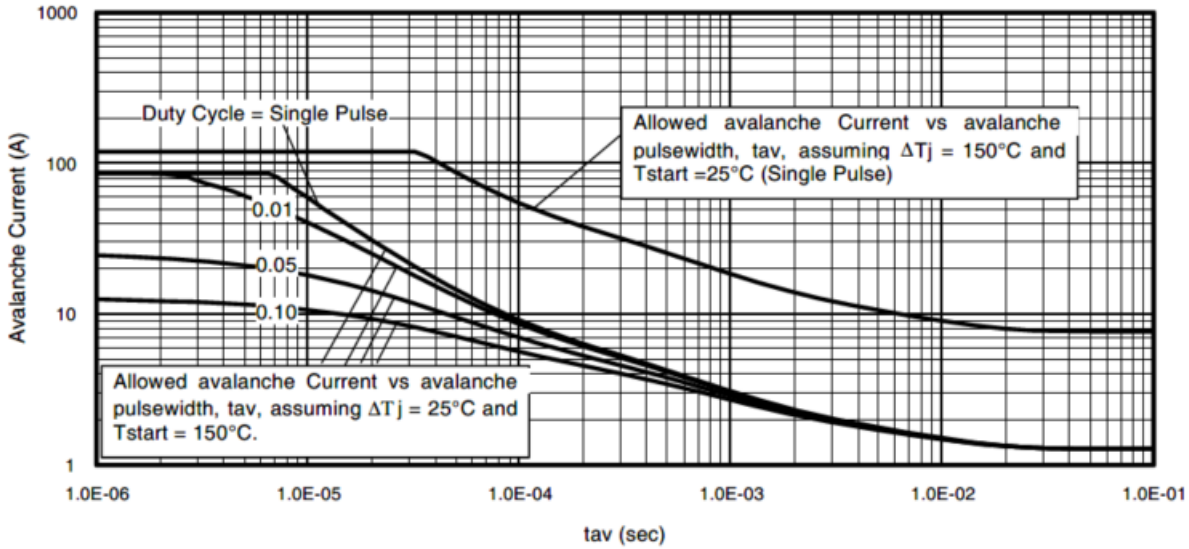


Fig 14. Typical Avalanche Current vs. Pulsewidth

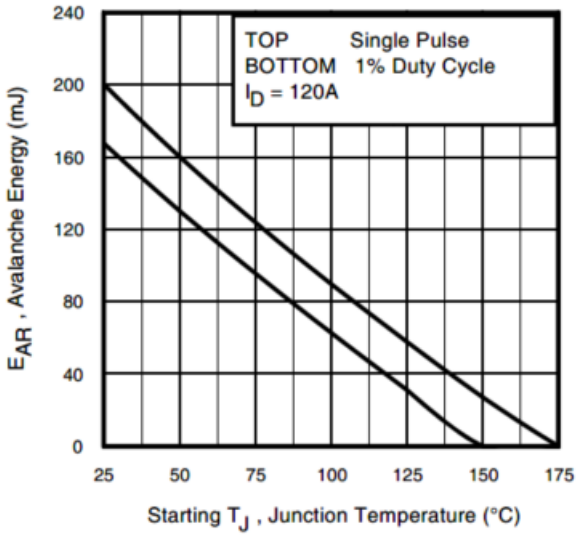


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

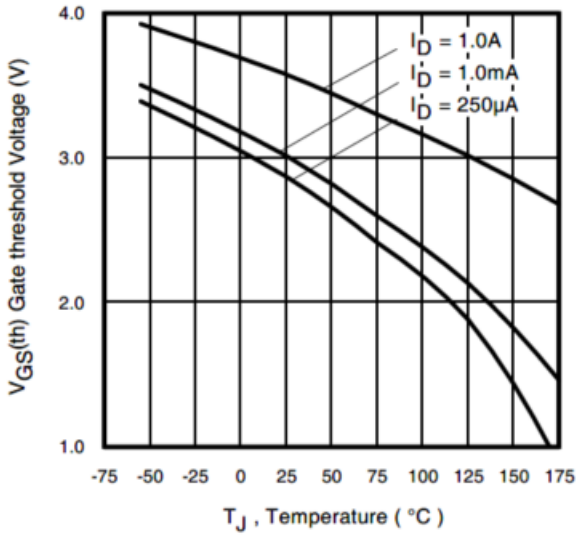


Fig. 16 Threshold Voltage vs. Temperature

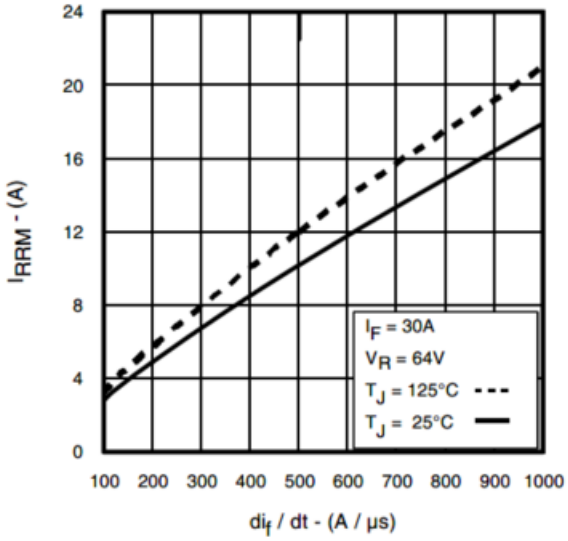


Fig. 17 Typical Recovery Current vs. di_f/dt

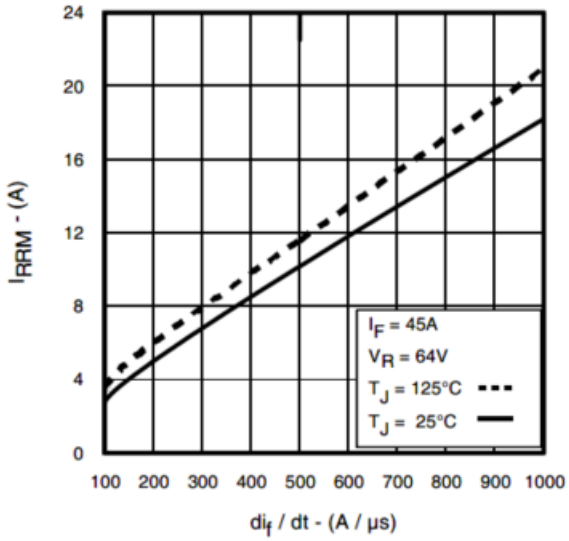


Fig 18. Typical Recovery Current vs. di_f/dt

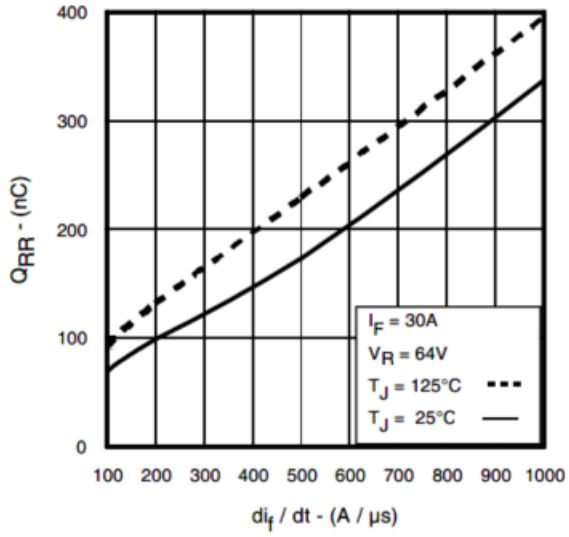


Fig 19. Typical Stored Charge vs. di_f/dt

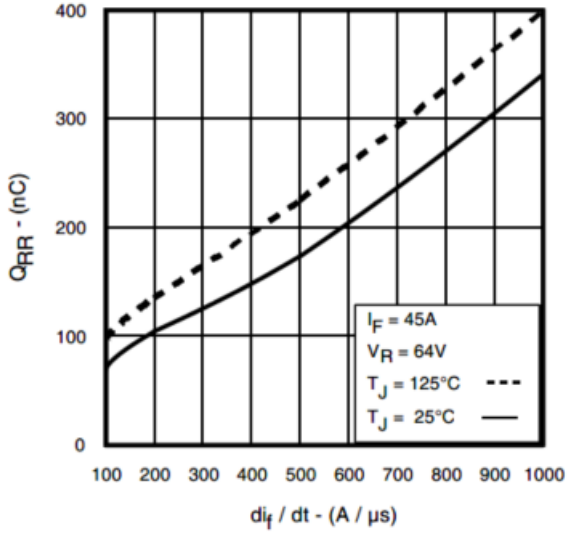


Fig 20. Typical Stored Charge vs. di_f/dt

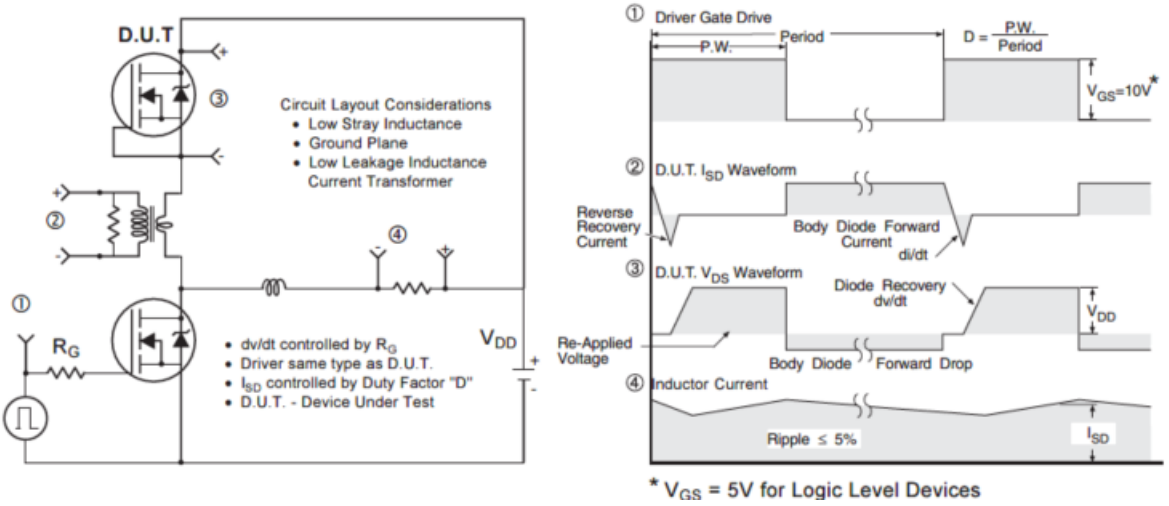


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

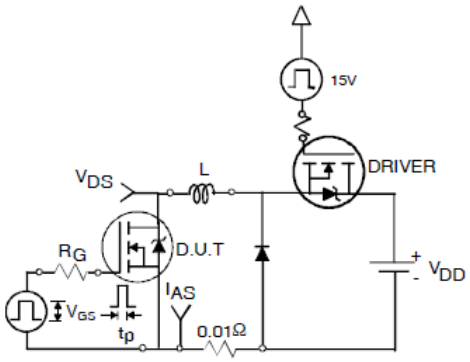


Fig 22a. Unclamped Inductive Test Circuit

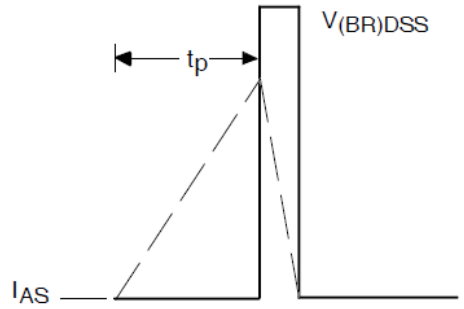


Fig 22b. Unclamped Inductive Waveforms

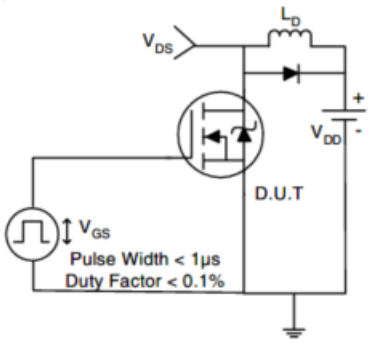


Fig 23a. Switching Time Test Circuit

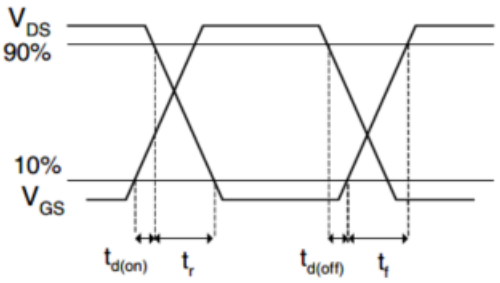


Fig 23b. Switching Time Waveforms

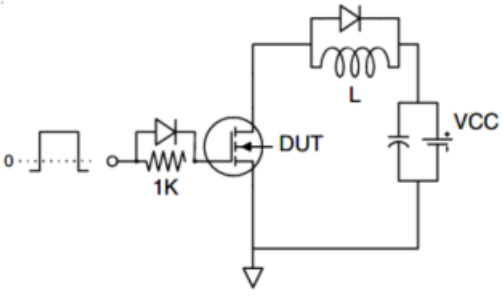


Fig 24a. Gate Charge Test Circuit

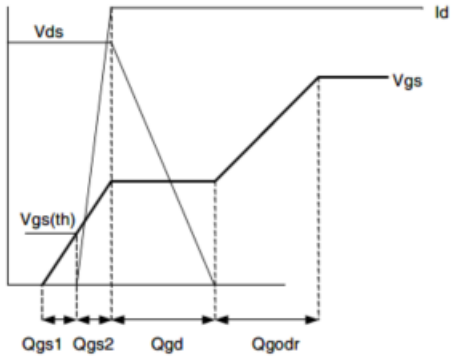
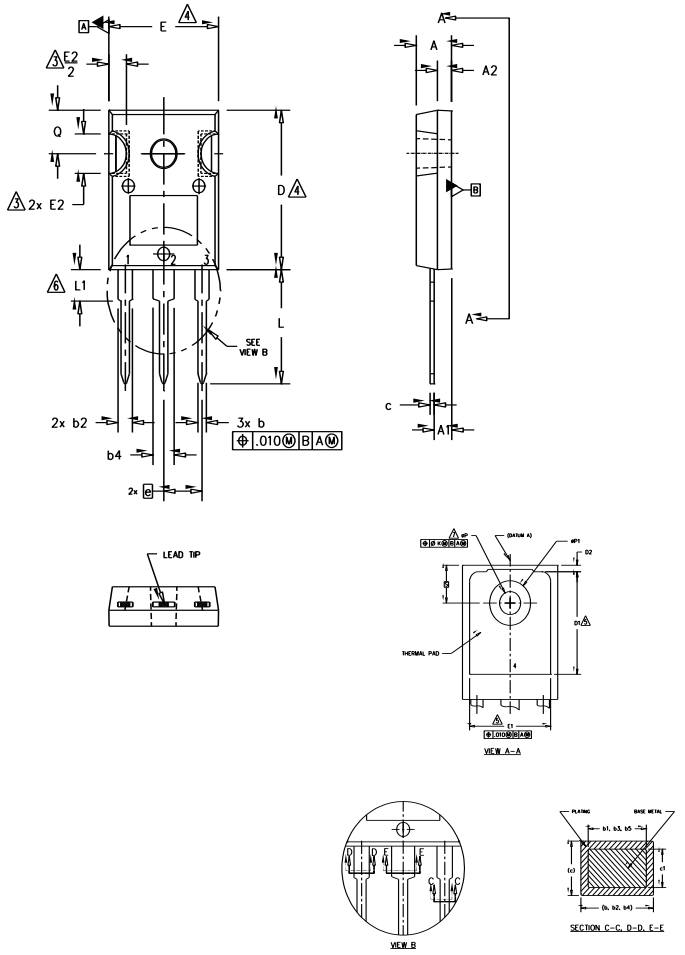


Fig 24b. Gate Charge Waveform

TO-247AC Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

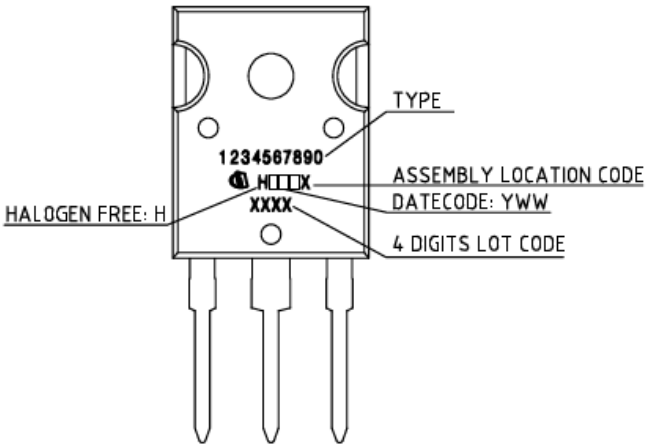
IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information



TO-247AC package is not recommended for Surface Mount Application.

Revision History

Date	Rev.	Comments
2013-09-06	2.0	• Final data sheet
2024-12-04	2.1	• Update datasheet to Infineon format • Updated Part marking –page 8 • Added disclaimer on last page.

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