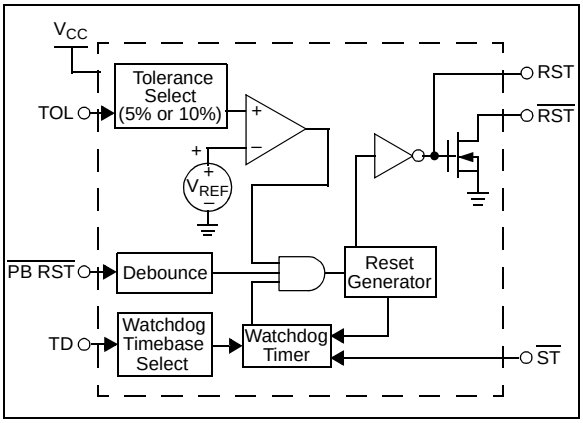
TC1232

Microprocessor Monitor

Features

- Precision Voltage Monitor
  - Adjustable +4.5V or +4.75V
- Reset Pulse Width – 250 msec minimum
- No External Components
- Adjustable Watchdog Timer
  - 150 msec, 600 msec or 1.2 sec
- Operating Voltage 4.0V to 5.5V
- Debounced Manual Reset Input for External Override

Block Diagram



General Description

The TC1232 is a fully-integrated processor supervisor that provides three important functions to safeguard processor sanity: precision power on/off reset control, watchdog timer and external reset override.

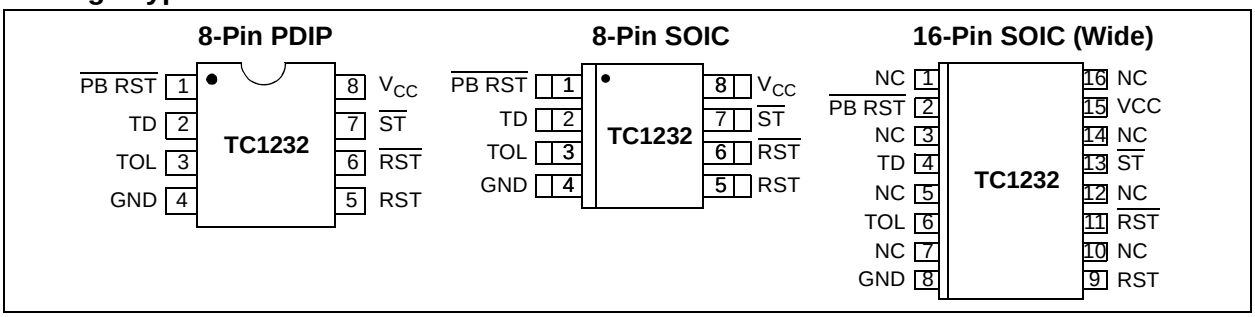
On power-up, the TC1232 holds the processor in the reset state for a minimum of 250 msec after V_{CC} is within tolerance to ensure a stable system start-up.

Microprocessor sanity is monitored by the onboard watchdog circuit. The microprocessor must provide a periodic low-going signal on the $\overline{ST}$ input. Should the processor fail to supply this signal within the selected time-out period (150 msec, 600 msec or 1200 msec), an out-of-control processor is indicated and the TC1232 issues a processor reset as a result.

The outputs of the TC1232 are immediately driven active when the PB input is brought low by an external push button switch or other electronic signal. When connected to a push button switch, the TC1232 provides contact debounce.

The TC1232 is packaged in a space-saving 8-Pin PDIP or SOIC package, a 16-Pin SOIC (wide) package and requires no external components.

Package Types



Device Features

Device	$\overline{RST}$ pin			RST pin		Trip Points (Max)	Minimum Reset Active Time (ms)	WDI Input Typical Timeouts (ms)	MR Input
	Type	Pull-up Resistor	Active Level	Type	Active Level				
TC1232	Open-drain	External	Low	Push-pull	High	4.75V or 4.5V	250	150, 600 or 1200	Yes

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Voltage on Any Pin (With Respect to GND) ..... -0.3V to +5.8V

Operating Temperature Range:

C-Version ..... 0°C to +70°C

E-Version..... -40°C to +85°C

Storage Temperature Range: ..... -65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{CC}	4.0	5.0	5.5	V	
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level	V_{IH}	2.0	—	V_{CC} +0.3	V	**Note 1**
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}	-0.3	—	+0.8	V	
Input Leakage $\overline{ST}$, TOL	I_L	-1.0	—	+1.0	µA	
Output Current RST	I_{OH}	-1.0	-12	—	mA	V_{OH} = 2.4V
Current RST, $\overline{RST}$	I_{OL}	2.0	10	—	mA	V_{OL} = 0.4V
Operating Current	I_{CC}	—	50	200	µA	Note 2
V_{CC} 5% Trip Point	V_{CCTP}	4.50	4.62	4.74	V	TOL = GND **(Note 3)**
V_{CC} 10% Trip Point	V_{CCTP}	4.25	4.37	4.49	V	TOL = V_{CC} **(Note 3)**
Capacitance Electrical Characteristics: Unless otherwise noted, T_A = +25°C**. (Note 4)**						
Input Capacitance $\overline{ST}$, TOL	C_{IN}	—	—	5	pF	
Output Capacitance RST, $\overline{RST}$	C_{OUT}	—	—	7	pF	

Note 1: $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40 kΩ.

2: Measured with outputs open.

3: All voltages referenced to GND.

4: Ensured by design.

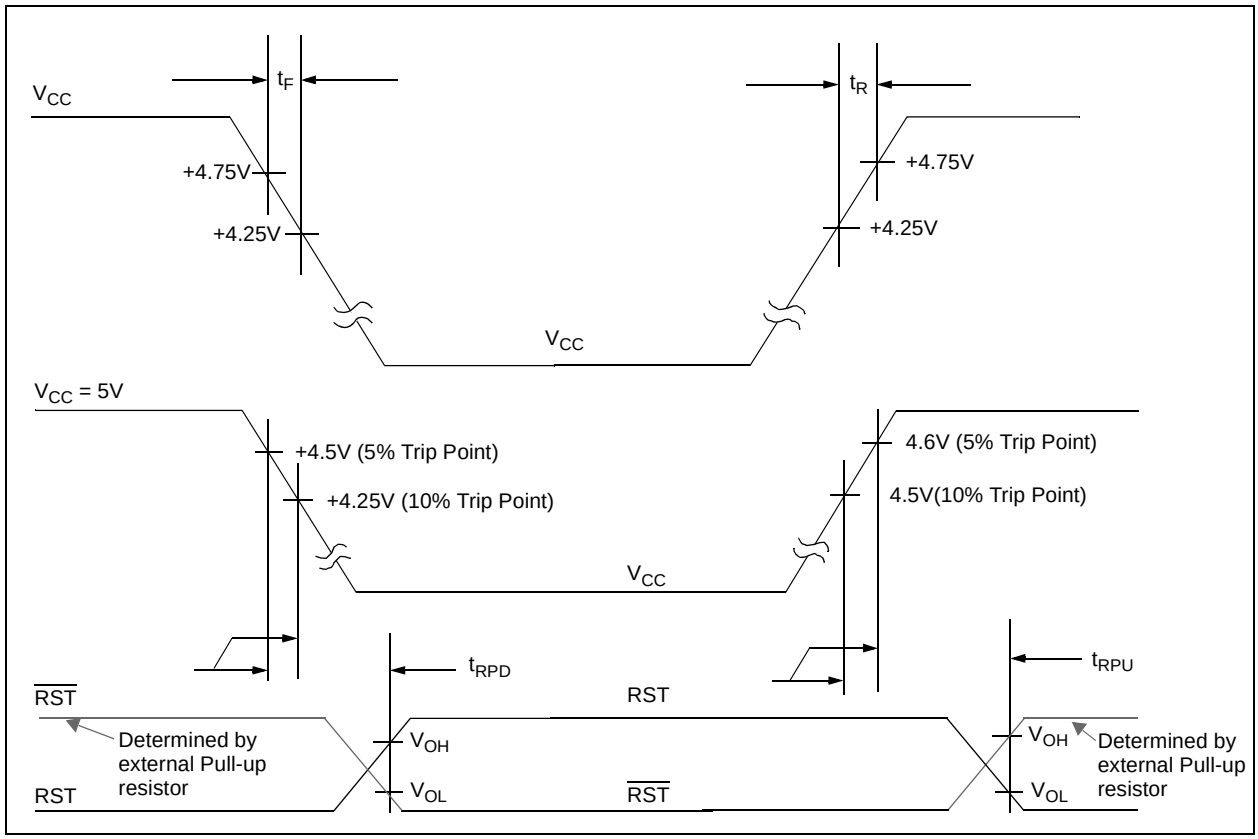


FIGURE 1-1: *Rise Time, Fall Time and Reset Detected to Reset Active Timing Waveforms.*

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{CC} Fall Time	t_F	10	—	—	µs	**Note 1**
V_{CC} Rise Time	t_R	0	—	—	µs	**Note 1**
V_{CC} Trip Point Detected to RST High and $\overline{RST}$ Low	t_{RPD}	—	—	100	ns	V_{CC} falling
V_{CC} Trip Point Detected to RST High and $\overline{RST}$ Open	t_{RPU}	250	610	1000	ms	V_{CC} rising **(Note 2)**

Note 1: Ensured by design.

2: t_R = 5 µs.

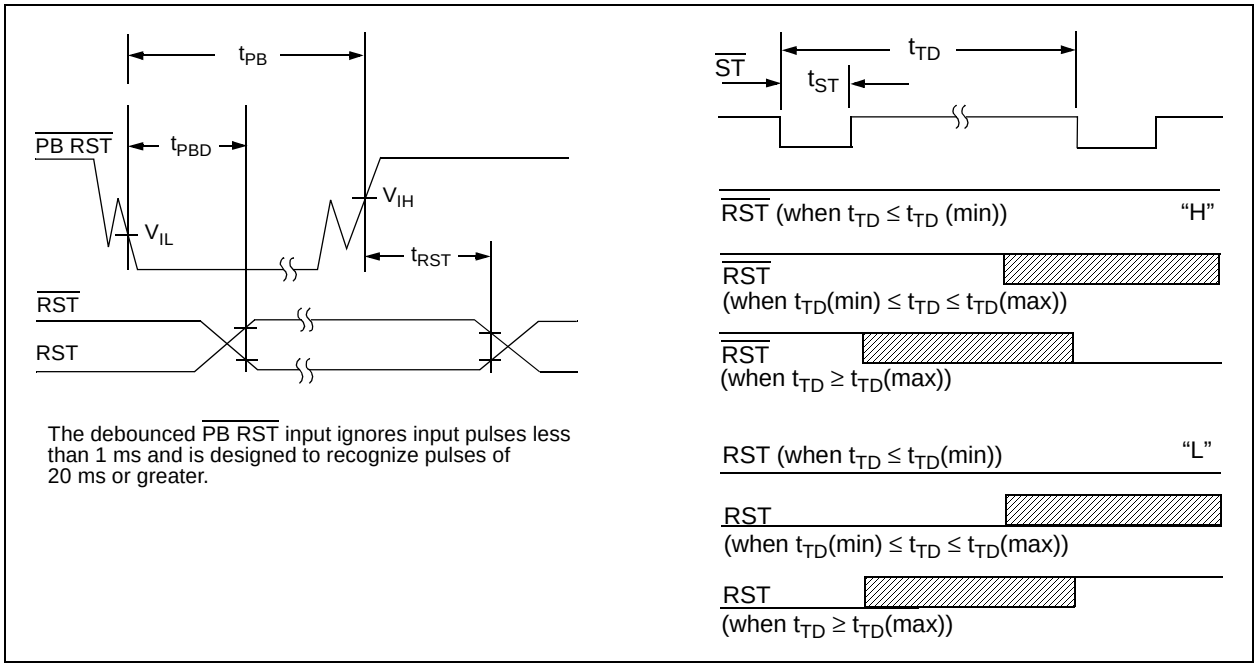


FIGURE 1-2: *Push Button Reset and Watchdog Timer Reset Timing Waveforms.*

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{PB RST}}$ Pulse Width	t_{PB}	20	—	—	ms	**Note 1**
$\overline{\text{PB RST}}$ Falling Edge Low to Reset Active	t_{PBD}	1	4	20	ms	
$\overline{\text{PB RST}}$ Rising Edge High to Reset Inactive	t_{RST}	250	610	1000	ms	
$\overline{\text{ST}}$ Pulse Width	t_{ST}	20	—	—	ns	
$\overline{\text{ST}}$ Time-out Period	t_{TD}	62.5	150	250	ms	TD Pin = 0V
		250	600	1000	ms	TD Pin = Open
		500	1200	2000	ms	TD Pin = V_{CC}

Note 1: $\overline{\text{PB RST}}$ must be held low for a minimum of 20 ms to ensure a reset.

2.0 TYPICAL PERFORMANCE CURVES

Performance Graphs are not available.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLES

Pin No.		Symbol	Pin Type	Buffer/ Driver Type	Function
8-pin PDIP, SOIC	16-pin SOIC				
1	2	$\overline{\text{PB RST}}$	I	ST	Push-button Reset Input. Input for a Manual Reset Switch. This input debounces (ignores) pulses less than 1 ms in duration and is ensured to recognize inputs of 20 ms or greater. L = Manual Reset Switch is Active, Force RST/$\overline{\text{RST}}$ pins Active H = Manual Reset Switch is Inactive. State of RST/$\overline{\text{RST}}$ pins determined by other system conditions.
2	4	TD	I	ST	Time Delay Input. The voltage level on this input determines the watchdog timer time-out period. TD = 0V $\rightarrow t_{TD}$ = 150 ms TD = Open $\rightarrow t_{TD}$ = 600 ms TD = V_{CC} $\rightarrow t_{TD}$ = 1.2 sec
3	6	TOL	I	ST	Tolerance Input. TOL = GND, Max Voltage Trip Point (V_{CCTP}) = 4.75V (5% tolerance) TOL = V_{CC}, Max Voltage Trip Point (V_{CCTP}) = 4.5V (10% tolerance)
4	8	GND	—	P	The ground reference for the device.
5	9	RST	O	Push Pull	Reset Output (Active-High) Goes active (High) if one of these conditions occurs: 1. If V_{CC} falls below the selected reset voltage threshold. 2. If $\overline{\text{PB RST}}$ pin is forced low. 3. If $\overline{\text{ST}}$ pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up
6	11	$\overline{\text{RST}}$	O	Open Drain	Reset Output (Active-Low) Goes active (Low) if one of these conditions occurs: 1. If V_{CC} falls below the selected reset voltage threshold. 2. If $\overline{\text{PB RST}}$ pin is forced low. 3. If $\overline{\text{ST}}$ pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up
7	13	$\overline{\text{ST}}$	I	ST	Strobe Input Input for Watchdog Timer. WDT period determined by state of TD pin Falling Edge $\rightarrow$ Resets Watchdog Timer counter (no time-out)
8	15	V_{CC}	—	P	The positive supply (+5V) for the device.
—	1,3,5, 7,10,12,16	NC	—	—	No internal connection.

4.0 OPERATIONAL DESCRIPTION

4.1 Power Monitor

The TC1232 provides the function of warning the processor of a power failure. When V_{CC} is detected as being below the voltage levels defined by the TOL pin, the TC1232's comparator outputs the RST and $\overline{RST}$ signals to a logic level that warns the system of an out-of-tolerance power supply. The RST and $\overline{RST}$ signals switch at a threshold value of 4.5V if TOL is tied to V_{CC}, and at a value of 4.75 volts if TOL is grounded. The RST and $\overline{RST}$ signals are held active for a minimum of 250 ms to ensure that the power supply voltage has been stabilized.

Figure 4-1 shows the V_{CC} fall time.

Figure 4-2 shows the V_{CC} rise time.

Figure 4-3 shows the time from when the voltage trip point is detected to the reset output pin going active.

Figure 4-4 shows the time from when the voltage trip point is exited to the reset output pin going inactive.

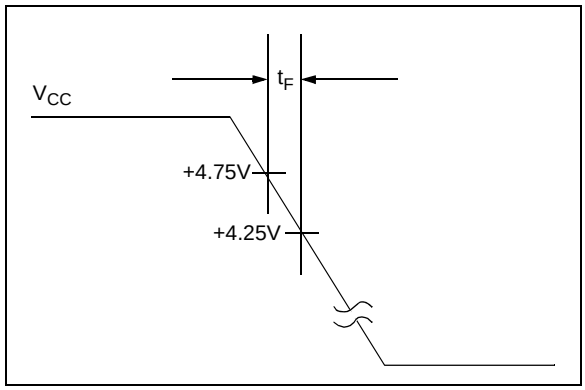


FIGURE 4-1: *Power-Down Slew Rate.*

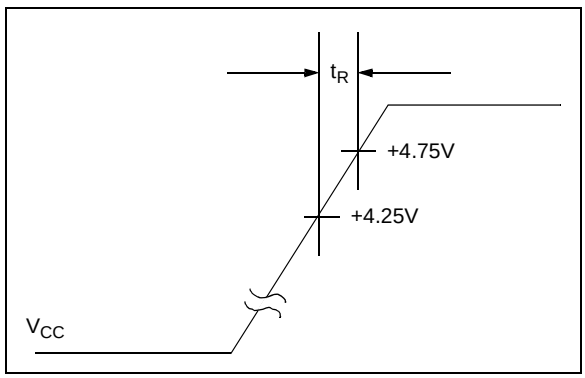


FIGURE 4-2: *Power-up Slew Rate.*

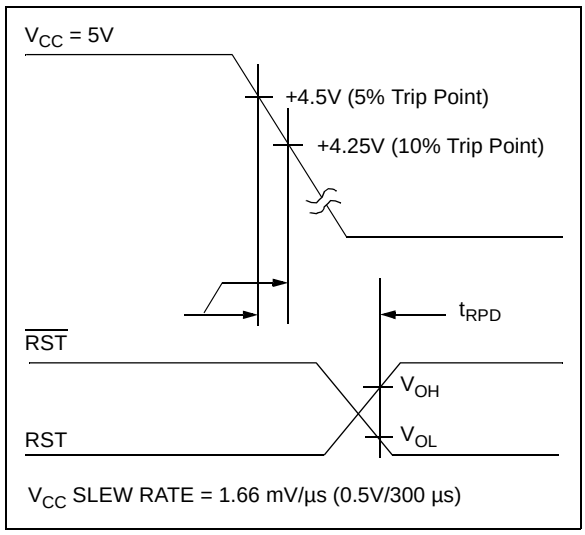


FIGURE 4-3: *V_{CC} Detect Reset Output Delay (Power-Down).*

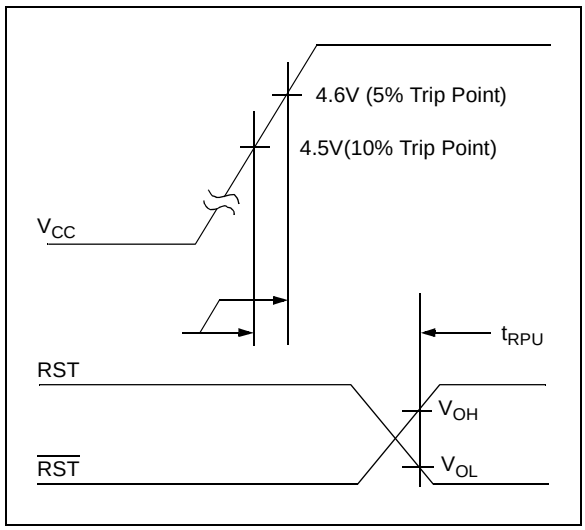


FIGURE 4-4: *V_{CC} Detect Reset Output Delay (Power-Up).*

4.2 Push Button Reset Input

The debounced manual reset input ($\overline{\text{PB RST}}$) manually forces the reset outputs into their active states. Figure 4-5 shows a block diagram for using the TC1232 with a push button switch.

Once $\overline{\text{PB RST}}$ has been low for a time t_{PBD} (the push-button delay time), the reset outputs go active. The reset outputs remain in their active states for a minimum of 250 ms after $\overline{\text{PB RST}}$ rises above V_{IH}. Figure 4-6 shows a waveform for the push button switch input and the reset pins output.

A mechanical push button or active logic signal can drive the $\overline{\text{PB RST}}$ input. The debounced input ignores input pulses less than 1 ms and recognizes pulses of 20 ms or greater. No external pull-up resistor is required because the $\overline{\text{PB RST}}$ input has an internal pull-up to V_{CC} of approximately 100 µA.

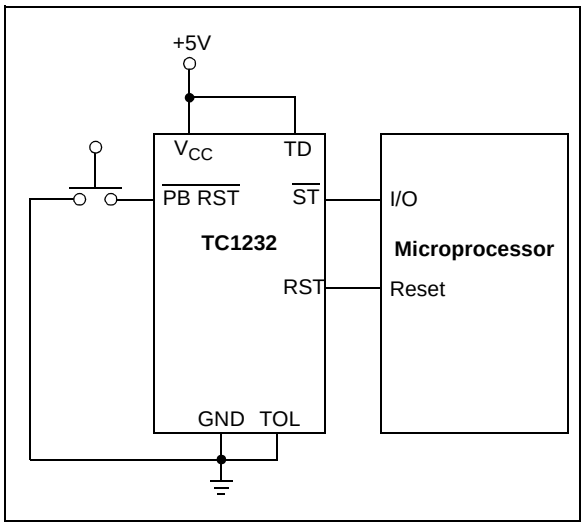


FIGURE 4-5: *Push Button Reset and Watchdog Timer.*

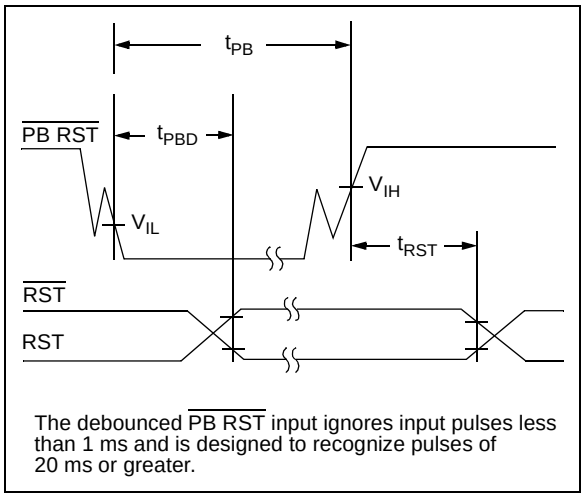


FIGURE 4-6: *Push Button Reset – $\overline{\text{PB RST}}$ Input.*

4.3 Watchdog Timer

When the $\overline{ST}$ input is not stimulated for a preset time period, the watchdog timer function forces RST and $\overline{RST}$ signals to the active state. The preset time period is determined by the $\overline{TD}$ inputs to be 150 ms with TD connected to ground, 600 ms with TD floating or 1200 ms with TD connected to V_{CC} (typ.). The watchdog timer starts timing-out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, the RST and $\overline{RST}$ signals are driven to the active state for 250 ms, minimum (Figure 4-7).

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that is executed frequently enough so the time between toggles is less than the watchdog time-out period. One common technique controls the microprocessor I/O line from two sections of the program. The software might set the I/O line high while operating in the Foreground mode and set it low while in the Background or Interrupt modes. If both modes do not execute correctly, the watchdog timer issues reset pulses.

t_{TD} is the maximum elapsed time between $\overline{ST}$ high-to-low transitions ($\overline{ST}$ is activated by falling edges only), which will keep the watchdog timer from forcing the reset outputs active for a time of t_{RST}. t_{TD} is a function of the voltage at the TD pin, as tabulated below:

TABLE 4-1: WATCHDOG TIMER PERIODS

Condition	t_{TD}		
	Min	Typ	Max
TD pin = 0V	62.5 ms	150 ms	250 ms
TD pin = Open	250 ms	600 ms	1000 ms
TD pin = VCC	500 ms	1200 ms	2000 ms

Figure 4-7 shows a block diagram for using the TC1232 with a PICmicro® MCU and the Watchdog input.

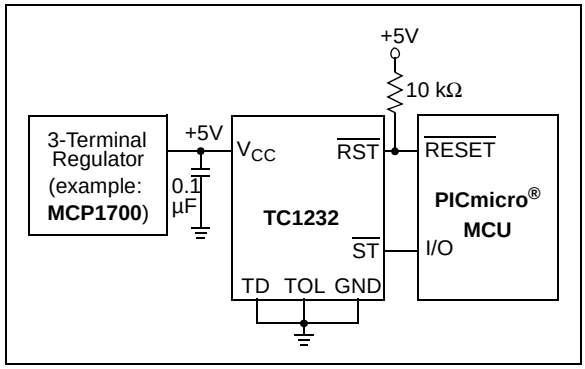


FIGURE 4-7: *Watchdog Timer.*

Figure 4-8 shows the expected reset output pin waveforms depending on the period of the $\overline{ST}$ pin falling edge and the state of the TD input pin.

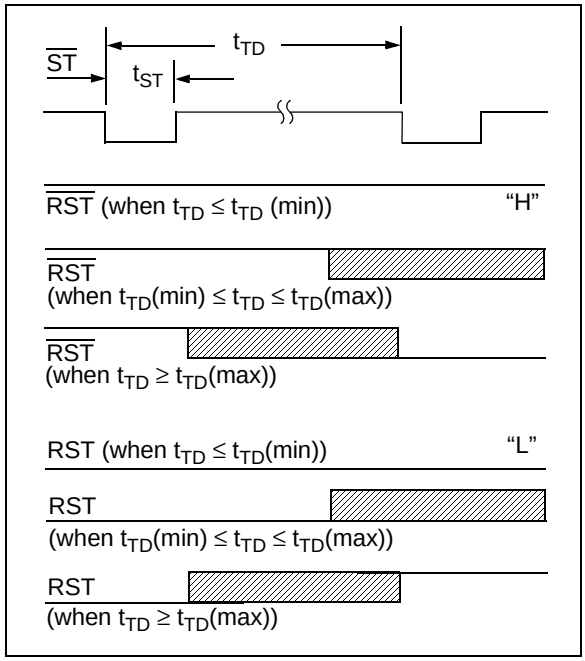


FIGURE 4-8: *Strobe Input.*

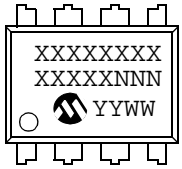
4.4 Supply Monitor Noise Sensitivity

The TC1232 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays) may require a 0.01 µF or 0.1 µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC1232 as possible to keep the capacitor lead length short.

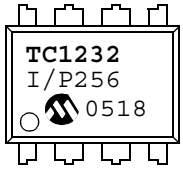
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

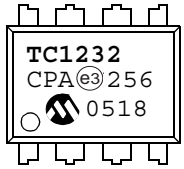
8-Lead PDIP (300 mil)



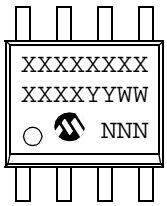
Examples:



OR

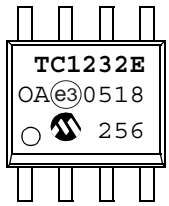


8-Lead SOIC (150 mil)

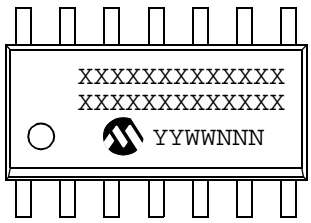


Examples:

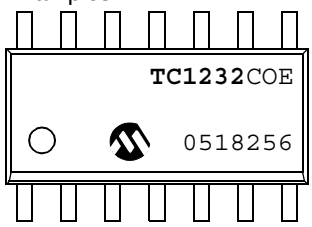
OR



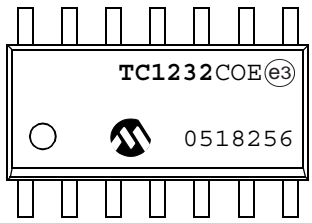
16-Lead SOIC (150 mil)



Examples:



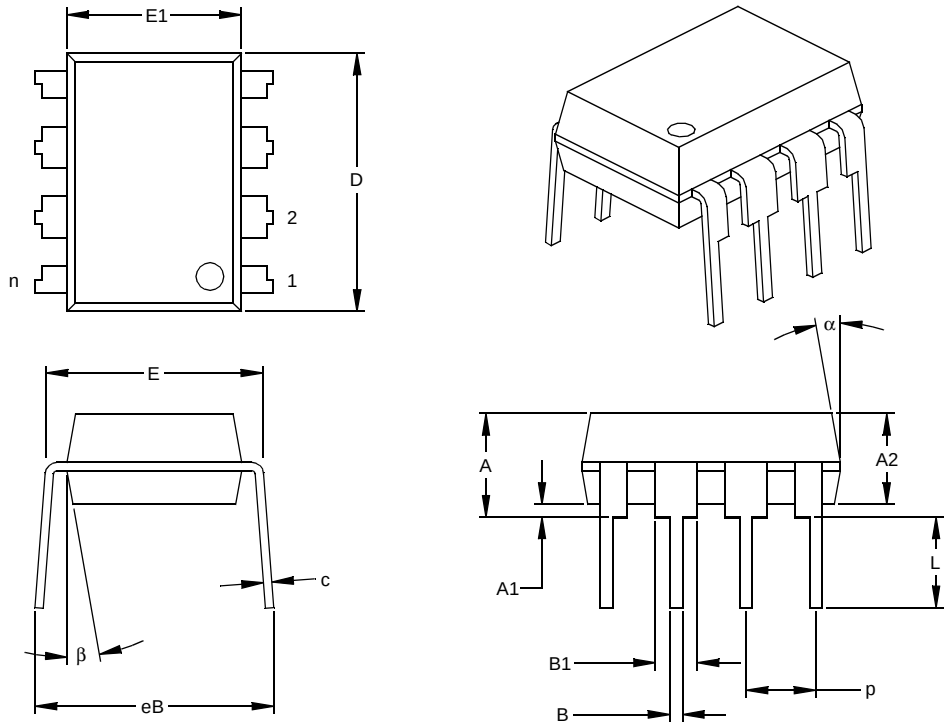
OR



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

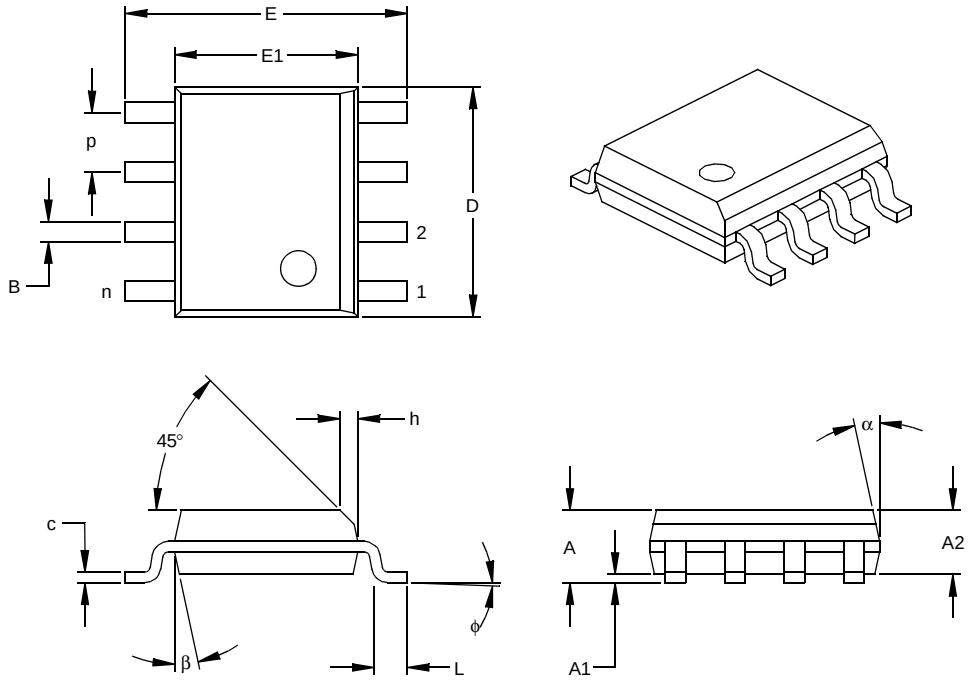


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

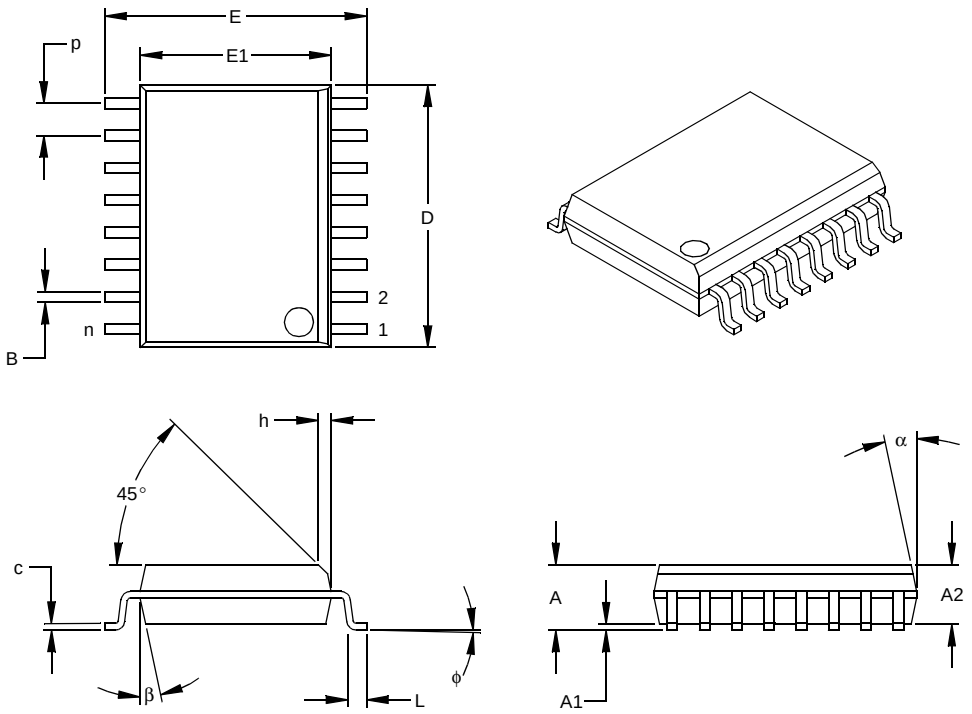


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

16-Lead Plastic Small Outline (OE) – Wide, 300 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.398	.406	.413	10.10	10.30	10.49
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-102

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (June 2005)

The following is the list of modifications:

1. Since no data is given in **Section 2.0 "Typical Performance Curves"**, "Preliminary" was added to the bottom of this document.
2. Corrected Operating Voltage in the Electrical Specifications
3. General Data Sheet Enhancements
4. Added Revision History Appendix Section

Revision B (March 2003)

- Not logged

Revision A (March 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC1232:	Microprocessor Monitor
Temperature Range:	C =	0°C to +70°C
	E =	-40°C to +85°C
Package:	PA =	Plastic DIP (300 mil Body), 8-lead
	OA =	Plastic SOIC, (150 mil Body), 8-lead
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead Tape and Reel
	OE =	Plastic SOIC (300 mil Body), 16-lead
	OE713 =	Plastic SOIC (300 mil Body), 16-lead Tape and Reel

Examples:

a) TC1232COA: 0°C to +70°C, 8L-SOIC

b) TC1232COA713: 0°C to +70°C, 8L-SOIC, Tape and Reel

c) TC1232COE: 0°C to +70°C, 16L-SOIC

d) TC1232COE713: 0°C to +70°C, 16L-SOIC Tape and Reel

e) TC1232CPA: 0°C to +70°C, 8L-PDIP

f) TC1232EOA: -40°C to +85°C, 8L-SOIC

g) TC1232EOA713: -40°C to +85°C, 8L-SOIC, Tape and Reel

h) TC1232EOE: -40°C to +85°C, 16L-SOIC

i) TC1232EOE713: -40°C to +85°C, 16L-SOIC, Tape and Reel

j) TC1232EPA: -40°C to +85°C, 8L-PDIP

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Qingdao
Tel: 86-532-502-7355
Fax: 86-532-502-7205

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

Japan - Kanagawa
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel:011-604-646-8870
Fax:011-604-646-5086

Philippines - Manila
Tel: 011-632-634-9065
Fax: 011-632-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Taiwan - Hsinchu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria - Weis
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Ballerup
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Massy
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Ismaning
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

England - Berkshire
Tel: 44-118-921-5869
Fax: 44-118-921-5820

04/20/05

