RVPW016 Current Mode PWM Controller

4-100VIN WIDE INPUT RANGE

FEATURES

- 4V to 100V Wide Input Range
- Suitable for Flyback/Buck/Boost and other Topologies
- Current Limit Threshold Voltage is 156mV
- Single Resistor Programmable Oscillator
- The Oscillator Frequency Decreases linearly with the Lower Load at Light Load State for efficiency
- Skip Cycle Mode for Low & No-load Power Consumption
- The Quiescent Current of Off-state is only 0.1uA
- Cycle-by-Cycle OCP/SCP/OTP
- Inner Leading Edge Blanking
- Inner Slope Compensation
- Accurately adjustable UVLO with Hysteresis
- Inner or External Soft Start(Optional)
- Converter that is set to PSR also can work in CCM/DCM due to Inner Gain and Phase Compensator
- Optocoupler can be connected directly to port for constituting a Feedback Loop
- MSOP10 Package

APPLICATIONS

- DCM/CCM Flyback Converters
- Converter for Industrial Power Supplies
- BMS Auxiliary Power Supplies
- POE Power Supplies
- Telecom Power Supplies

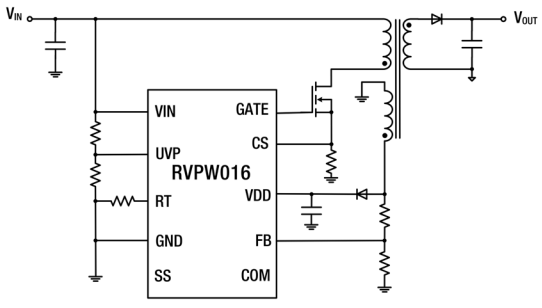
DESCRIPTION

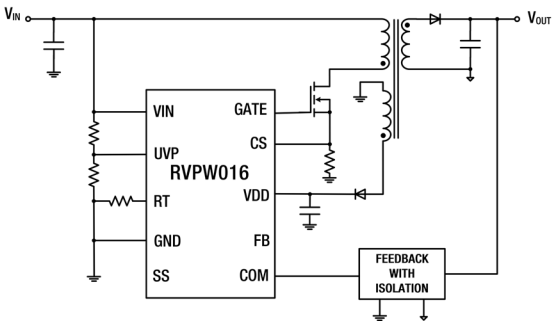
RVPW016 is a highly integrated DC-DC controller designed to support a wide range of power conversion topologies and output voltage feedback methods. It features an integrated start-up circuit that accommodates an ultra-wide input voltage range from 4V to 100V. To prevent reverse current flow, an internal diode blocks current from flowing back from VDD to VIN. An internal differential amplifier is employed for current sampling, significantly enhancing the signal-to-noise ratio (SNR). The current-sensing threshold voltage is set at 156mV, effectively balancing performance with low power consumption in the current detection circuitry. To reduce system cost and improve reliability, the design eliminates the need for a current transformer. Under heavy-load conditions, the RVPW016 operates at the maximum switching frequency, which is programmable via an external resistor. As the load decreases, the controller linearly reduces the switching frequency to maintain high efficiency. This adaptive frequency scaling also minimizes both light-load output ripple and no-load power consumption. The device supports Primary-Side Regulation (PSR) at operating frequencies up to several hundred kilohertz. Its internal output voltage sampling circuit is compatible with both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), with a minimum sampling pulse width of 350ns. A built-in loop compensator with fast dynamic response enhances the stability and transient performance of the system. To ensure high system reliability, the RVPW016 incorporates precisely adjustable undervoltage lockout (UVLO) with hysteresis, as well as output short-circuit protection(SCP), output overvoltage protection(OVP), and over-temperature protection(OTP).

Device information

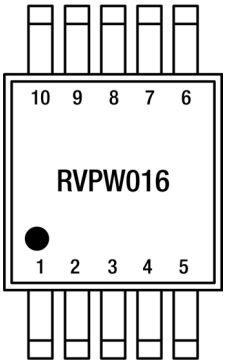
Part Number	Package	Dimension	SPQ
RVPW016	MSOP10	3.0mm*4.9mm	5000

SIMPLIFIED SCHEMATIC





PIN CONFIGURATION AND FUNCTIONS



Name	No.	Type	Description
COM	1	SSR	Optocoupler feedback pin. The voltage on COM adjusts peak current and frequency. An internally integrated RC compensator allows direct connection to an optocoupler.
VIN	2	---	The input of start up circuit. A high-voltage LDO connects VIN and VDD. The regulated VDD voltage is 8.6V, capable of providing a maximum load current of 20mA.
UVP	3	---	Input under-voltage protection pin. The comparison threshold voltage is 2V. The UVP circuit sinks 4.4μA from the UVP pin to GND when active. A pull-up resistor sets the UVP hysteresis.
VDD	4	---	Power supply port of device, it has a clamp protection circuit. The clamping voltage is 18.6V. When the current sunk by the clamp circuit exceeds 6.6mA, device will enter a self-recovery protection mode.
GATE	5	---	Connect this pin to the gate of the external MOSFET.
GND	6	---	System ground.
CS	7	---	Current sense input, the CS threshold voltage of RVPW016 is 156mV. It has short-circuit protection function, when the voltage of CS is greater than 1.6 times the threshold voltage, the device will enter a self-recovery protection mode.
RT	8	---	The pin for setting frequency. An external resistor connected from this pin to GND sets the oscillator frequency.
SS	9	---	Soft-start timing pin. An external capacitor from this pin to GND sets the soft-start time. If left floating, the soft-start time defaults to 0.72ms.
FB	10	PSR	Feedback pin. The device continuously monitors the FB pin for a negative voltage while the GATE is high or COM is connected to GND. If detected, the device automatically selects FB as the sampling voltage feedback pin.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN to GND	V_{IN}	-0.3	110	V
The continuous current of clamped VIN	$I_{VIN(CLAMP)}$		1	mA
VDD and GATE to GND	V_{DD}	-0.3	25	V
All other pins to GND		-0.3	6.6	V
Junction Temperature	T_{JMAX}		150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2023; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

Recommended Operatings Conditions

		MIN	NOM	MAX	UNIT
VIN Supply Voltage	V_{IN}	4		100	V
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

VIN=12V or VDD=12V and T=25°C, unless otherwise indicated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN						
$I_{VIN(SHDN)}$	Shutdown current	V_{UVP}=0V		0.1		uA
$I_{VIN(UVP)}$	VIN current under UVP	V_{UVP}=1.8V		294		uA
I_Q	Supply current	GATE is suspended, 3.3kΩ is connected from COM to GND		2.0	3.0	mA
$I_{VIN(SRC)}$	Power supply capability	V_{IN}=12V, V_{DD}=6.5V	15	20		mA
$V_{IN(clamp)}$	ESD clamp voltage	I_{VIN}=1mA, V_{DD}=12V	110	118	128	V
VDD						
$V_{DD(ON)}$	VDD turn on threshold	V_{DD} rising	3.5	3.7	3.9	V
$V_{DD(OFF)}$	VDD turn off threshold	VDD falling	3.2	3.4	3.6	V
$V_{DD(REG)}$	VDD regulated voltage	V_{DD} and GATE are No-load	8.1	8.7	9.3	V
$V_{DD(DO)}$	Drop voltage of the LDO	$I_{VDD(SNK)}$=5mA, V_{IN}=8V		1.2		V
$V_{BV(DIODE)}$	Break voltage of Diode		37			V
$V_{DD(OVP)}$	Threshold voltage of OVP	V_{DD} rising	17.5	18.6	19.7	V
$I_{DDSNK(OVP)}$	Absorbed current of OVP	V_{DD}= $V_{DD(OVP)}$		6.6		mA
$V_{DD(clamp)}$	ESD clamp voltage	$I_{VDD(SNK)}$=10mA	23	27		V
CS						
$t_{CS(DLY)}$	Current limit comparison delay	The time interval from CS becomes 0.6V to GATE becomes low level		40		nS
$V_{CS(LIM)}$	Current limit maximum threshold voltage		140	156	172	mV
$V_{CS(MIN)}$	Current limit minimum threshold voltage	PSR	26	31	36	mV
$V_{SCP(LIM)}$	Short-circuit protection threshold voltage	V_{COM}>$V_{COM(OLP)}$	225	250	275	mV
$t_{CS(OVLD)}$	Clk cycle count under OCP			2^{14}		T_{sw}
$t_{REST(SR)}$	The rest time of OCP			400		mS
$t_{LEB(CS)}$	LEB time of CS			95		nS
$t_{LEB(SCP)}$	LEB time of SCP			50		nS
$D_{35\%}$	Initial duty cycle of slope compensation			35		%
SS						
$V_{SS(OPEN)}$	Open circuit voltage of soft start pin	CLK pin is suspended	5.0	5.4	5.8	V
$t_{SS(IN)}$	Inner soft start up time	COM as feedback, SS pin is suspended	0.3	0.72	1.1	mS
I_{SS}	External soft start current		22	28	34	uA
$R_{SS(DIS)}$	Bleeder resistor			300		Ω
$R_{SSTOCOM}$	Resistance from SS to COM			800		Ω
RT						
F_{OSC1}	Frequency at R_T=44.2kΩ		135	150	165	kHz
F_{OSC2}	Frequency at R_T=22kΩ		270	300	330	kHz
F_{OSC3}	Frequency at R_T=13.3kΩ		440	500	560	kHz
V_{RT}	Voltage of RT		1.92	2.02	2.12	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVP						
$V_{REF(UVP)}$	Reference voltage of UVP		1.9	2.0	2.1	V
$V_{UVP(CLAMP)}$	Clamp voltage of pin	I_{UVP}=0.6mA flow into UVP pin	5.0	5.5	6.0	V
$I_{UVP(SNK)}$	Current sucked from UVP	V_{UVP}=1.8V	3.4	4.4	5.4	uA
$V_{UVP(ON)}$	Voltage for LDO turn on	V_{UVP} is ascending		0.9		V
$V_{UVP(OFF)}$	Voltage for LDO turn off	V_{UVP} is descending		0.6		V
FB						
$V_{REF(REG)}$	Reference voltage of EA		1.975	2.000	2.025	V
A_V	Low frequency gain of EA			1400		V/V
$T_{D(SAMP)}$	Delay time of sampling	RT=22kΩ		252		nS
I_{FB}	Pin input current	FB as feedback pin		40		nA
		COM as feedback pin		-20		uA
COM						
D_{MIN}	Minimum duty cycle				0	%
D_{MAX}	Maximum duty cycle		75	80	85	%
K_{PWM}	Gain of COM to PWM comparator			0.42		
$V_{COM(OPEN)}$	Open circuit voltage		5.0	5.4	5.8	V
$V_{COM(OLP)}$	Threshold voltage of OLP	VDD≥5.4V		4.6		V
		VDD<5.4V		V_{DD}-0.8		V
I_{COM}	Short-circuit current	V_{COM}=0V	0.6	1.1	1.5	mA
$V_{COM(DMAX)}$	Pin voltage at maximum duty cycle			3.75		V
$V_{COM(SKIP)}$	Voltage when device enters skip mode			1.0		V
$V_{COM(HYS)}$	Hysteresis when device recovey from skip mode			8		mV
GATE						
V_{GATEH}	GATE with 50mA load, Voltage difference between VDD and VGATE when GATE outputs high level	I_{GATE}=50mA		185		mV
V_{GATEH}	Voltage at low level which provides 100mA pull-up current for GATE	I_{GATE}=100mA		170		mV
$I_{GATE(SRC)}$	Maximum soucre current	V_{GATE}=7.5V		0.8		A
$I_{GATE(SINK)}$	Maximum sink current	V_{GATE}=7.5V		1.5		A
t_r	Rise Time	1nF Cap is connected to GND		30		nS
t_r	Fall Time	1nF Cap is connected to GND		20		nS
OTP						
T_{SHDN}	Threshold Temperature		148	163	178	°C
$T_{SHDN(HYS)}$	Hysteresis Temperature			18		°C

Typical Characteristics

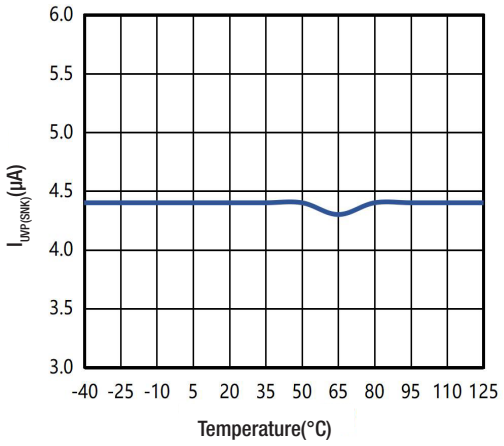


Fig. 1 $I_{UVP(SNK)}$ vs Temperature

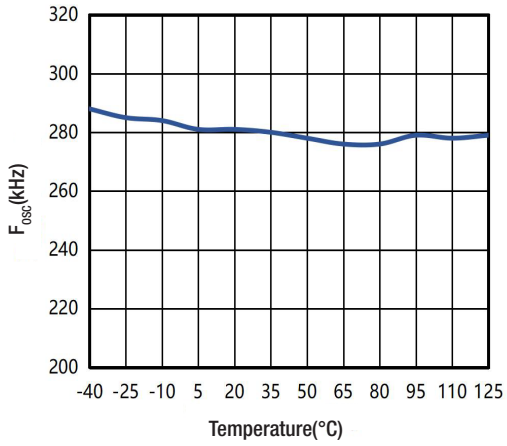


Fig. 2 F_{OSC} vs Temperature@R_T=22kΩ

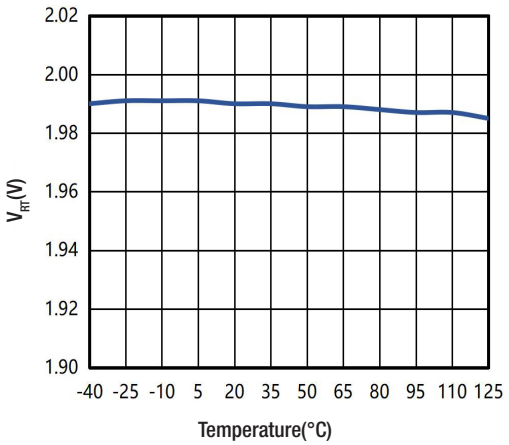


Fig. 3 V_{RT} vs Temperature

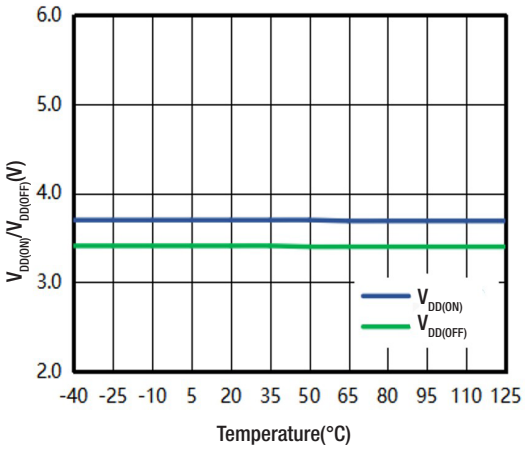


Fig. 4 $V_{DD(ON)}$/$V_{DD(OFF)}$ vs Temperature

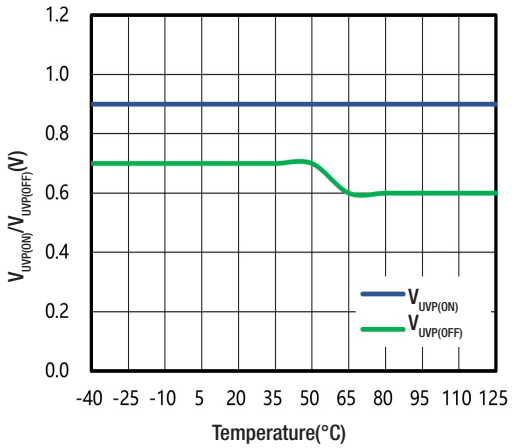


Fig. 5. $V_{UVP(ON)}$/$V_{UVP(OFF)}$ vs Temperature

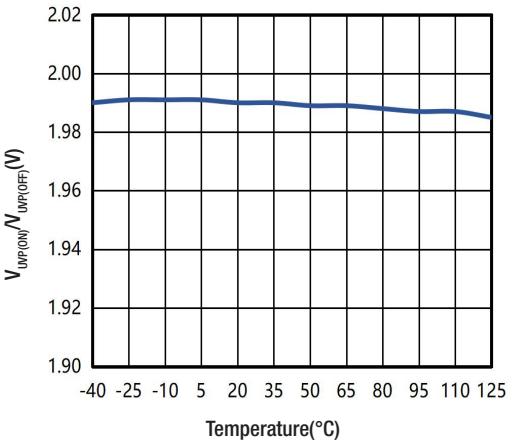


Fig. 6. $V_{REF(REG)}$ vs Temperature

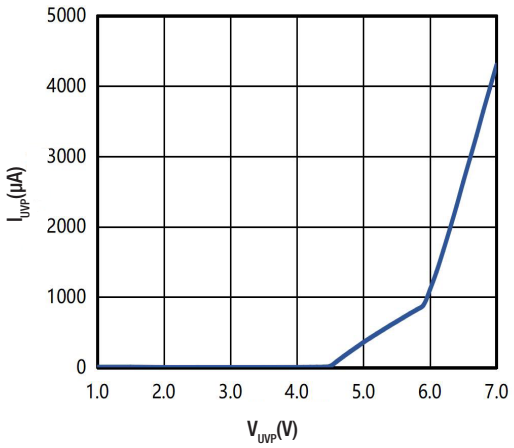


Fig. 7. I_{UVP} vs V_{UVP}

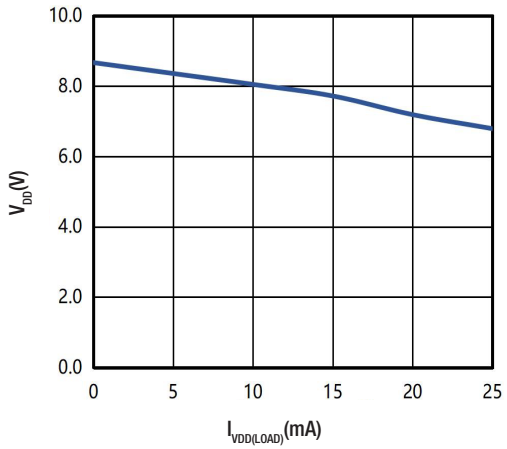


Fig. 8. V_{DD} vs $I_{VDD(LOAD)}$

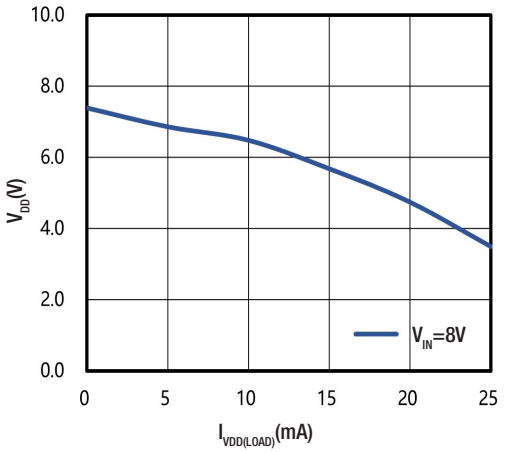


Fig. 9. V_{DD} vs $I_{VDD(LOAD)}$

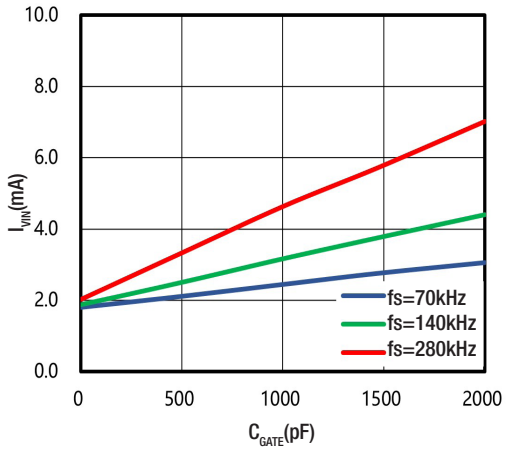


Fig. 10. I_{VIN} vs C_{GATE}

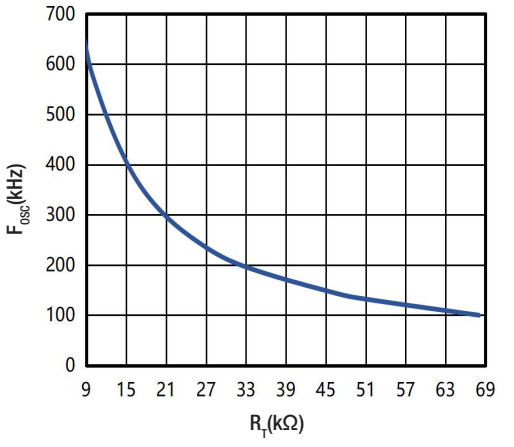


Fig. 11. F_{OSC} vs R_T

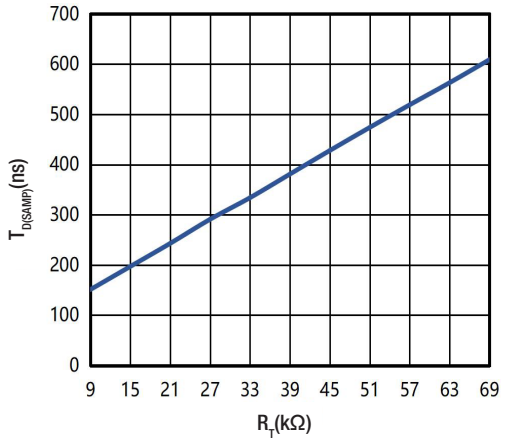


Fig. 12. $T_{D(SAMP)}$ vs R_T

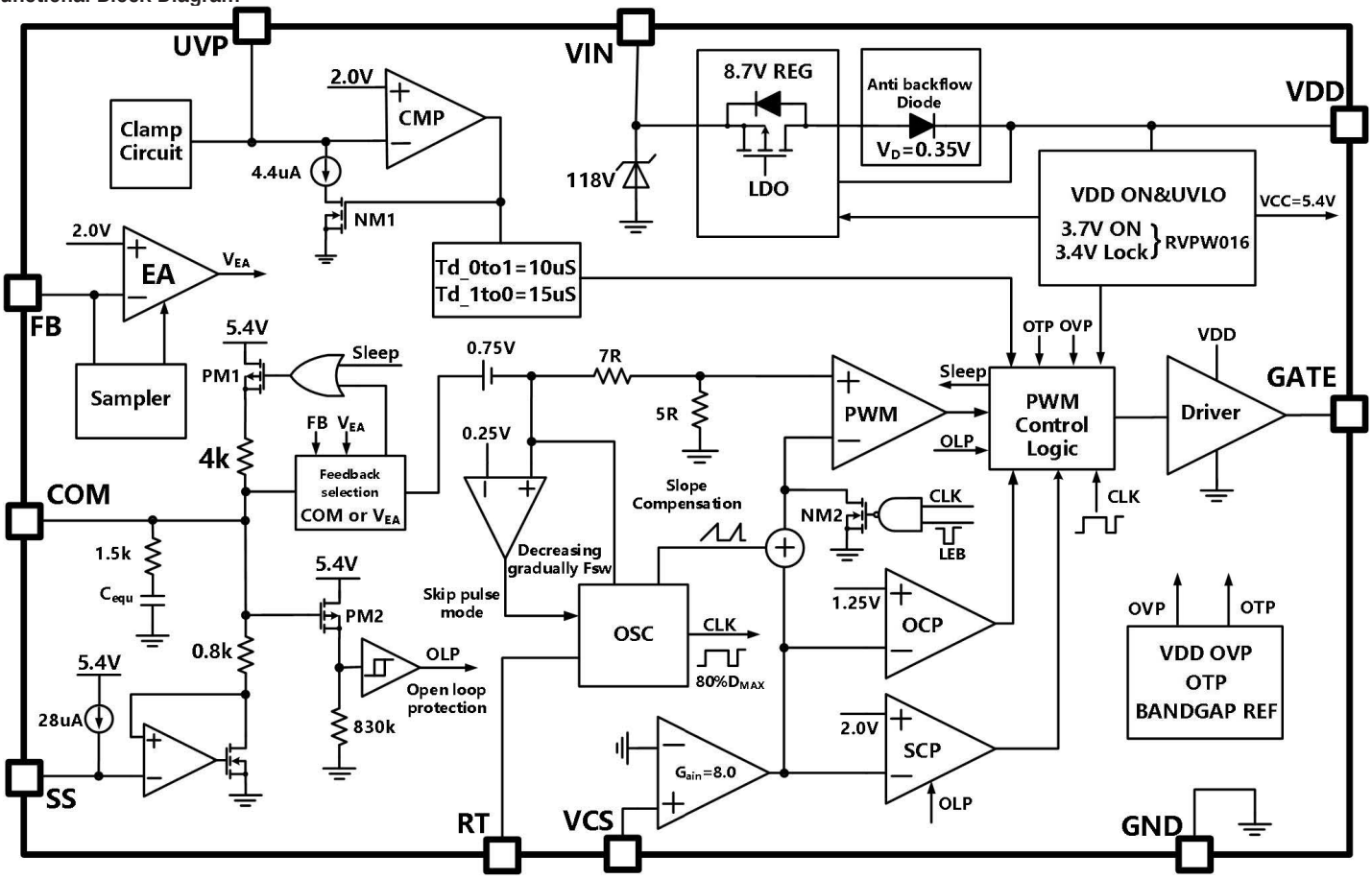
DETAILED DESCRIPTION

Overview

RVPW016 series are highly integrated, current-mode PWM controllers suitable for a wide range of topologies, including Flyback, Buck, and Boost converters. They feature an integrated high-voltage start-up circuit, and an internal diode prevents reverse current from flowing from VDD to VIN, simplifying the design of the external start-up circuitry. An internal differential amplifier is used for current sensing, significantly enhancing the signal-to-noise ratio (SNR) and enabling ultra-low threshold current detection for improved control precision. RVPW016 series support multiple feedback loop methods. Among them, high-speed sampling circuit for Primary-Side Regulation (PSR) enables the design of no-optocoupler switching power supplies operating at frequencies of several hundred kHz. This allows for reduced system cost, improved reliability, and simplified isolation design.

A programmable soft-start function allows users to define the start-up duration to minimize inrush current and reduce output overshoot. The integrated slope compensation circuit helps prevent subharmonic oscillation in peak current mode. Each protection function is equipped with built-in filtering to eliminate the impact of transient interference signals. When protection is triggered, the device automatically shuts down unnecessary internal modules to reduce power consumption. Under ultra-light load conditions, the controller enters an extremely low-frequency operation mode. This mode significantly reduces no-load power consumption while maintaining low output voltage ripple, thereby improving standby efficiency. RVPW016 series also provide comprehensive protection features to ensure reliable operation. The UVP pin allows users to configure the input undervoltage protection threshold and hysteresis. VDD pin is used to detect output overvoltage conditions. The COM pin enables detection of output overload and open-loop faults, while the CS pin provides short-circuit protection for both the output and the transformer.

Functional Block Diagram



Feature Description

Start-up and Power Supply

A low-dropout (LDO) linear regulator is integrated between the high-voltage VIN pin and the low-voltage VDD pin. The operation of this LDO is controlled by the UVP pin: the LDO is enabled when the UVP voltage exceeds 0.9V and disabled when the voltage falls below 0.6V. When the LDO is turned off, the power consumption is extremely low, with the drain current of the internal MOSFET reduced to the nanoampere (nA) level. To protect the LDO from damage due to high-voltage transients, an ESD clamp diode is placed at the VIN pin. In cases where the VIN voltage may briefly exceed the clamp voltage (e.g., during input surges), it is recommended to place a resistor between the VIN pin and the positive input voltage rail to improve system reliability. LDO output voltage is fixed at 8.7V and can supply a maximum load current of 20mA. If the VDD voltage rises above 8.7V, the LDO automatically shuts off. A Schottky diode is connected in series between VIN and VDD to prevent reverse current flow from VDD to VIN. This prevents current from flowing through the parasitic diode of the PMOS transistor inside the LDO when VDD exceeds VIN.

The VDD pin includes voltage clamping and overvoltage protection features. The clamp voltage is set at 18.6V, and overvoltage protection is triggered when the current drawn by the clamping circuit exceeds 6.6mA, placing the device into protection mode. In flyback converter applications, the rectified auxiliary winding of the transformer can be used to supply power to the VDD pin. This approach not only improves power conversion efficiency but also enables output overvoltage protection. This is because the voltage on the auxiliary winding is directly proportional to the secondary output voltage of the transformer, allowing the VDD overvoltage protection circuit to effectively detect and respond to output overvoltage events.

CS, OCP, SCP

RVPW016 amplifies the voltage at the CS pin using an internal proportional differential amplifier with a fixed gain of 8. The amplified CS voltage is then used as the input signal for both the Overcurrent Protection (OCP) and Short-Circuit Protection (SCP) comparators. Given that the reference voltages for the OCP and SCP comparators are 1.25V and 2.00V, respectively, the corresponding threshold voltages at the CS pin are 156mV for OCP and 250mV for SCP. Overcurrent Protection (OCP) is implemented in a cycle-by-cycle manner. When the CS pin voltage exceeds the OCP threshold (156mV), the GATE output immediately stops driving the external power MOSFET high. Additionally, if the CS voltage continues to exceed 156mV for 2^{14} consecutive switching cycles, the device enters a fault condition, recognizing that the load demand exceeds the maximum current limit. In this case, the RVPW016 enters protection mode and automatically recovers after a 400ms delay.

Short-Circuit Protection (SCP) is triggered when either a high voltage at the COM pin (used in open-loop feedback) or a high output voltage from the EA block (when FB is used in feedback) is detected. Under such conditions, the SCP comparator becomes active. If the CS voltage exceeds 250mV, the device enters protection mode and recovers automatically after 400ms. To prevent false triggering due to noise, especially during the switching of the external power MOSFET, the RVPW016 integrates a Leading Edge Blanking (LEB) circuit. The LEB period is 95ns, during which the amplified CS signal is blocked from reaching the PWM comparator, thus ignoring any transient noise spike.

For applications where the noise pulse width is longer than 95ns, it is recommended to implement an external RC filter at the CS pin. The filter capacitor should be placed as close as possible to the CS pin to maximize noise suppression and ensure accurate current sensing.

Various Voltage Feedback Mode

RVPW016 supports multiple feedback configurations for closed-loop control of the switching power supply. It can operate in secondary-side feedback mode using optocoupler isolation, primary-side regulation (PSR), or direct voltage sampling via a resistor divider. For secondary-side feedback, the control loop is introduced through the COM pin. For the latter two methods-primary-side and direct sampling-the output voltage of the converter is sensed through the FB pin. The appropriate feedback mode is automatically selected based on the peripheral circuitry during the first 12 switching cycles following power-up or exit from a protection state. If the COM pin is identified as the feedback input, its voltage is used directly as the duty cycle modulation voltage for the internal PWM comparator. Alternatively, if the FB pin is recognized as the feedback input, the output voltage of the internal error amplifier (EA) is used for modulation. For different feedback methods, the connection method of device pins is as follows:

Feedback mode	COM pin	FB pin
SSR by optocoupler	is connected to optocoupler	Float
PSR by winding	Float	is connected to resistor divider of auxiliary winding
Resistor divider	is connected to GND	is connected to resistor divider of output of converter

PWM Comparator

PWM comparator in the RVPW016 modulates the duty cycle of the GATE output by comparing the current sense voltage with a duty cycle modulation voltage. The modulation voltage is selected automatically after mode detection and is either the voltage at the COM pin or the output voltage of the internal Error Amplifier (EA), depending on the feedback configuration. This modulation voltage is first offset by 0.75V and then scaled using a 12:5 division ratio to produce the non-inverting input voltage of the PWM comparator. The voltage at the CS pin, used for current sensing, is amplified through a proportional differential amplifier and serves as the inverting input of the comparator. Additionally, a slope compensation voltage is superimposed on the amplified CS voltage to improve system stability. When the EA output voltage (from the FB pin) is used for modulation, the non-inverting input of the PWM comparator is subject to a minimum voltage limit of $V_{PWM(MIN)}$=250mV. This constraint corresponds to a minimum peak current sense threshold of $V_{CS(MIN)}$=31mV, ensuring a minimum on-time and stable operation at low load. In contrast, when the COM pin is used for modulation (secondary-side feedback), the PWM comparator imposes no minimum limit on the non-inverting input voltage. Therefore, the minimum conduction time can theoretically approach zero. In practice, it is primarily limited by the leading-edge blanking (LEB) time and the turn-off delay of the external power MOSFET.

RVPW016 supports a maximum PWM duty cycle of 80%. To prevent subharmonic oscillation when the duty cycle exceeds 50%, an internal slope compensation circuit is employed. A ramp signal is generated using the oscillator's ramp voltage and is applied through a slope compensation resistor, connected in series between the output of the current sense amplifier and the input of the PWM comparator. To minimize the negative impact of slope compensation on load capacity under low input voltage conditions, slope compensation is only activated when the duty cycle exceeds 35%. It remains disabled when the duty cycle is below 35%. At the maximum duty cycle of 80%, the voltage drop across the slope compensation resistor reaches 250mV.

Frequency Setting and Virtually Decreasing

Oscillator frequency of the RVPW016 is programmable using an external resistor connected to the RT pin. A constant reference voltage of 2V is maintained at the RT pin, which generates a reference current through the external resistor R_T. This current directly determines the charge and discharge rate of the internal relaxation oscillator, thereby setting the operating frequency of the controller. The oscillator frequency is thus inversely proportional to the resistance value of R_T. The formula for calculating the frequency is:

$$F_{osc} = \frac{6600}{R_T(k\Omega)}(kHz)$$

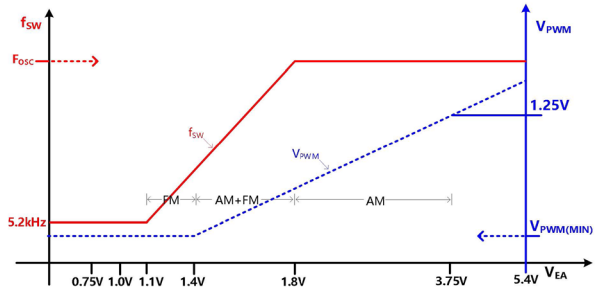


Fig. 13 Variation Curves of Switching Frequency and Peak Current with V_{EA}

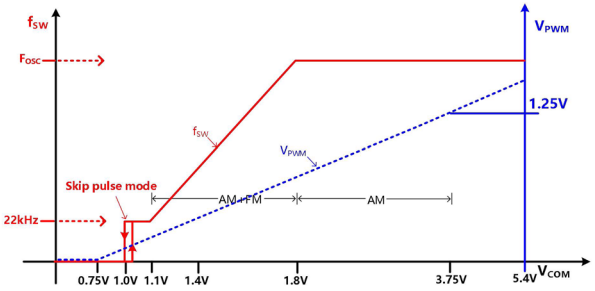


Fig. 14 Variation Curves of Switching Frequency and Peak Current with V_{COM}

RVPW016 includes a virtual frequency reduction function that gradually decreases the switching frequency as the converter load decreases. This dynamic frequency scaling significantly improves efficiency under light-load conditions. When operating under ultra-light or no-load conditions, the device employs different strategies based on the selected feedback mode to minimize power consumption. In primary-side regulation (PSR) mode, burst-mode operation is not supported; therefore, the minimum switching frequency is limited to 5.2kHz. To ensure stability and prevent output voltage drift, a dummy load is recommended at the output to absorb the minimum power delivered. In contrast, when configured for secondary-side regulation (SSR) mode, the converter is allowed to enter burst mode. If burst mode is not desirable in SSR applications, it can be suppressed by increasing the voltage at the CS pin-either by adding feedforward compensation or by drawing a small current from the VDD pin. Additionally, whenever the GATE pin outputs a switching pulse, the pulse frequency always exceeds 22kHz, which helps eliminate audible noise during operation.

Setting threshold and hysteresis of UVP

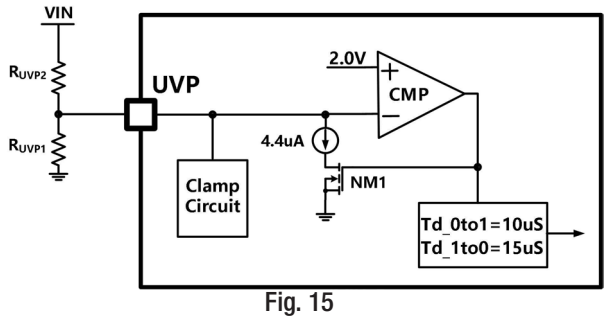


Fig. 15

UVP pin of the RVPW016 is used to configure the input under-voltage lockout (UVLO) threshold. By selecting an appropriate external resistor divider, both the UVLO threshold voltage and its hysteresis can be accurately set. In addition to its UVLO function, the UVP pin also serves as an ON/OFF control input. When UVP is pulled low, the internal LDO is disabled, and the device's power consumption drops significantly-limited only to the drain leakage current of the internal MOSFET, typically in the nanoampere (nA) range.

When the UVP pin voltage falls below 2V, the device generates a shutdown control signal. If this condition persists for at least 10μs, the controller enters a protection state. Recovery from this protection occurs only if the UVP voltage rises above the threshold for at least 15μs, providing immunity to transient noise and preventing false UVLO triggering. For applications requiring a longer filtering time constant, a capacitor may be connected from the UVP pin to ground. While in the protection state, the device sources a 4.4μA pull-down current at the UVP pin. This current, flowing through the upper resistor in the divider R_{UVP2}, creates a defined voltage hysteresis between UVLO shutdown and recovery thresholds. Additionally, the UVP pin includes an internal clamp: if the UVP voltage exceeds 4.0V, the clamping circuitry activates to absorb excess current and prevent overstress. The input voltage-current characteristics of this clamp behavior are illustrated in Figure 7. The input undervoltage protection threshold voltage and recovery voltage can be calculated using the following formula:

$$V_{IN(UVP+)} = \frac{2V \times (R_{UVP1} + R_{UV2})}{R_{UVP1}} + 4.4\mu A \times R_{UVP2}$$

$$V_{IN(UVP-)} = \frac{2V \times (R_{UVP1} + R_{UV2})}{R_{UVP1}}$$

Soft start up

Soft-start function of the RVPW016 ensures that the output voltage and transformer excitation current gradually ramp up to their steady-state values during power-up. This controlled start minimizes inrush current and reduces electrical stress on the components during startup. When the COM pin is selected as the feedback input, an internal current source generates a 28μA charging current that flows into the SS pin, charging the external soft-start capacitor C_{SS}. The voltage rise across C_{SS} determines the ramp-up rate of the COM voltage, thereby controlling the rate of increase in the PWM duty cycle. By adjusting the value of the external capacitor C_{SS}, the user can program the desired soft-start duration to suit the specific application requirements.

PSR using FB pin for voltage feedback

RVPW016 senses the output voltage of the switching power supply via the auxiliary winding of the transformer. A resistor divider connected from the auxiliary winding to the FB pin enables voltage sampling during the transformer's demagnetization stage. During this phase, the sampled voltage is applied to the inverting input of the internal error amplifier (EA), while a fixed reference voltage, $V_{REF(REG)}$=2V, is applied to the non-inverting input. The EA amplifies the difference between these two voltages to produce a modulation voltage, V_{EA}, which determines the duty cycle of the converter. As illustrated in Figure 16, this V_{EA} output modulates the switching behavior of the power supply. The auxiliary winding voltage waveform referenced in the operation is shown in Figure 17. Once the feedback loop stabilizes, the sampled voltage at the FB pin equals the internal reference voltage of 2V, enabling accurate output regulation. Based on this relationship, the following output voltage formula can be derived:

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_A}{N_S} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2V$$

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} \times 2V - (V_F + I_S R_S)$$

Output Voltage Sampling and Accuracy Considerations: In the transformer, N_S and N_A represent the turns of the secondary output winding and the primary auxiliary winding, respectively. R_{FB2} and R_{FB1} are the resistor dividers connected to the auxiliary winding for voltage sampling. V_F is the junction voltage drop of the output diode, I_S is the secondary winding output current, and R_S represents the total resistance of the secondary output circuit. From the output voltage expression, it is evident that the term $I_S R_S$ negatively affects load regulation accuracy. To mitigate this effect, the RVPW016 samples the FB pin voltage at the end of the transformer's demagnetization stage, where I_S is at its minimum. In Discontinuous Conduction Mode (DCM), I_S=0, meaning the output voltage is unaffected by the $I_S R_S$ term.

Therefore, for designs requiring high output voltage accuracy, DCM operation is recommended. In contrast, in Continuous Conduction Mode (CCM), the output voltage decreases as load increases due to the influence of $I_S R_S$. Regardless of conduction mode, RVPW016 detects the end of the transformer demagnetization stage based on a 20% sudden drop in FB voltage. When this drop occurs, the internal sampler latches the output of the differential amplifier (EA). Because EA has an intentional delay in its response, the latched voltage effectively reflects the FB voltage just prior to the drop, ensuring sampling accuracy. During the early stage of demagnetization-after the power transistor turns off-the FB voltage may oscillate significantly due to resonance between the transformer's leakage inductance and parasitic capacitance. To avoid false sampling, a sampling delay $T_{D(SAMP)}$ is implemented during which the sampler is inactive. Accurate sampling occurs only after this delay. During the active sampling period, the peak-to-peak amplitude of the FB resonance should be limited to within 20% (approximately 400 mV) of the FB platform voltage. Note that the voltage reflected to the auxiliary winding must be adjusted according to the resistor divider ratio. The sampling delay $T_{D(SAMP)}$ is related to the oscillator frequency set by the external R_T resistor. For example, when R_T=22kΩ, $T_{D(SAMP)}$≈252ns, as shown in Figure 16. To ensure accurate output voltage sensing, filter capacitors should not be placed in parallel with the FB pin to GND, as this may distort the FB waveform, especially in high-frequency PSR (Primary-Side Regulation) applications operating in the hundreds of kHz. Additionally, the parasitic capacitance of the oscilloscope probe can interfere with FB waveform integrity under light-load conditions due to shortened demagnetization time, potentially causing output voltage deviations. For optimal waveform fidelity and acceptable power consumption in the voltage divider network, R_{FB1} is recommended to be in the range of 2.5kΩ to 6kΩ, with a typical value of 4kΩ.

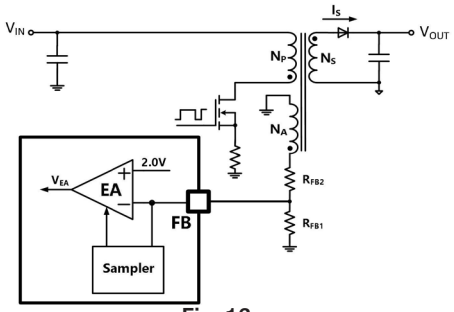


Fig. 16

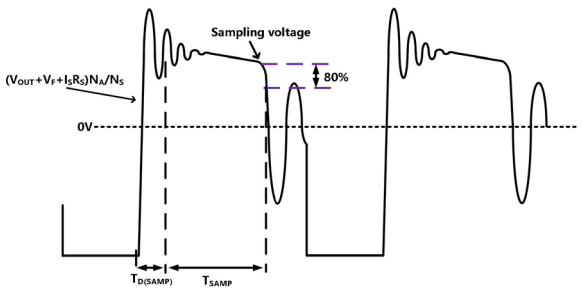


Fig. 17

Operation mode

Feedback Port and Soft Start Up

As shown in Figure 18, when the device is powered on or recovers from a protection shutdown, it enters the mode selection phase during the first 12 switching cycles (t_1 to t_2), followed by the soft start-up stage (t_2 to t_3). During the mode selection stage, the COM pin voltage is approximately 3.2V. This voltage is used solely for feedback mode detection and does not cause a high peak current at the CS pin, as the PWM comparator threshold is internally limited at this stage. If the COM pin is connected to an optocoupler, the 3.2V detection voltage persists for the full 12-cycle duration. However, if the FB pin is configured for Primary Side Regulation (PSR) feedback, the detection voltage duration shortens to only two cycles once mode selection concludes. In applications using optocoupler feedback, the soft start-up stage begins immediately after the mode selection phase. During soft start, the COM pin voltage is regulated by the SS pin. As the voltage on the SS pin gradually rises, the PWM duty cycle increases proportionally, ensuring a controlled and smooth startup.

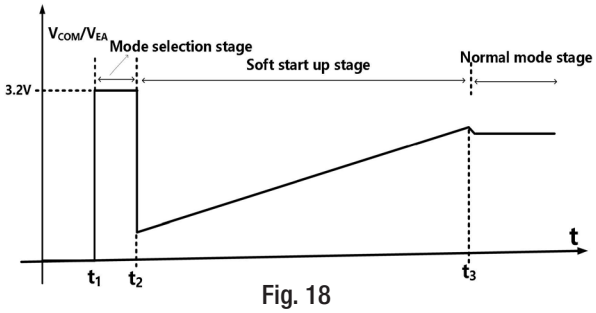


Fig. 18

Normal Operation State

When the voltages at the COM, CS, VDD, and UVP pins remain within their normal operating ranges and do not trigger any protection logic, the output voltage stabilizes and forms a closed-loop feedback at time t_3, as shown in Figure 18. At this point, the soft start-up phase is complete, and the device transitions into the normal loop regulation state. Depending on the output load conditions of the switching power supply at the end of the soft start-up t_3, the internal control voltage V_{COM}/V_{EA} reaches different levels and the device enters a steady-state operating mode. Under these conditions, the RVPW016 may operate at the oscillator's fixed switching frequency F_{OSC}, transition into a mode with gradually decreasing frequency, or enter burst mode operation when using SSR feedback.

Output Overload, SCP, OLP

Excessive output load, output short circuit, and open-loop conditions caused by poor soldering or damaged components are common fault scenarios in power systems. The RVPW016 integrates comprehensive protection and control mechanisms to address these abnormalities, as illustrated in Figure 19. Each of these conditions can lead to an abnormal rise in the duty cycle modulation voltage V_{COM} and V_{EA}. When this voltage exceeds the open-loop protection threshold of 4.6V (or V_{DD}–0.8V when V_{DD} is below 5.4V), the device initiates a protection timing sequence. This timing does not begin unless the modulation voltage exceeds the threshold continuously. During this phase, the duration of the GATE output pulse gradually increases, following the soft-start progression. If the modulation voltage remains above the threshold for 2^{14} consecutive switching cycles (with any interruption resetting the counter), the protection mechanism is triggered. At this point, the device enters a fault protection state with a 400ms interval. Before the 2^{14}-cycle count is reached, the protection mode may also be activated earlier by other conditions. For example, a short circuit protection (SCP) event may be triggered if the CS voltage becomes too high, or overvoltage protection may activate if V_{DD} exceeds 18.6V. Therefore, by analyzing the GATE pulse width, CS voltage, and V_{DD} voltage prior to the protection event, the specific fault condition-such as SCP, OVP, or open-loop-can be diagnosed, enabling efficient root cause analysis of the abnormal behavior.

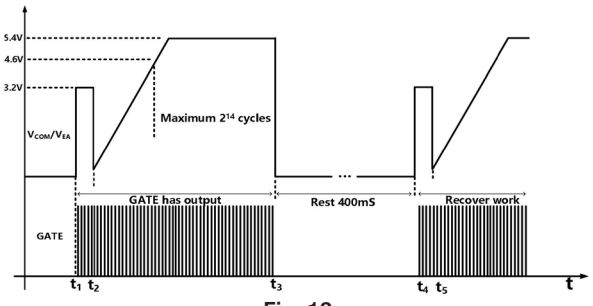


Fig. 19

APPLICATION AND IMPLEMENTATION

Application information

Start Up Circuit

As shown in Figure 20, the dashed boxes labeled ①, ②, ③, and ④ illustrate four different startup circuit connection methods, each optimized for specific input voltage ranges and application conditions.

① – In this method, the high-voltage pin (VIN) of the device is connected directly to the input of the switching power supply. The internal high-voltage LDO then generates power for the VDD pin. Based on the VIN pin's maximum voltage rating, this approach is suitable for input voltages up to 100V.

② – This configuration introduces a resistor between the VIN pin and the switching power supply input to suppress short-term voltage spikes. The resistor value typically ranges from several hundred to several thousand ohms, depending on the VDD current requirement under the minimum input voltage conditions.

③ – A Zener clamp voltage regulator circuit can be added externally to expand the high-voltage input capability of the RVPW016. In designs that do not utilize the VIN pin, a diode is typically connected between the startup transistor's emitter and the VDD pin to prevent reverse breakdown. However, due to the integrated anti-backflow Schottky diode between VIN and VDD within the RVPW016, this external diode is not required when using an external high-voltage startup circuit connected to VIN.

④ – With a startup threshold of 3.7V, the RVPW016 supports applications with input voltages as low as 4V. When powering the device directly from a low-voltage input, a power transistor with a gate threshold voltage below 1V should be selected to ensure reliable conduction, especially since the VDD voltage may momentarily drop once the converter begins operation. Alternatively, by connecting the cathode of the RCD snubber circuit's diode (located at the drain of the startup power transistor) to the RVPW016's VIN pin, the device can start up from input voltages as low as 4.5V without requiring a low-threshold MOSFET. After startup, the reflected voltage and leakage inductance energy sustain the device's operation by boosting the internal voltage.

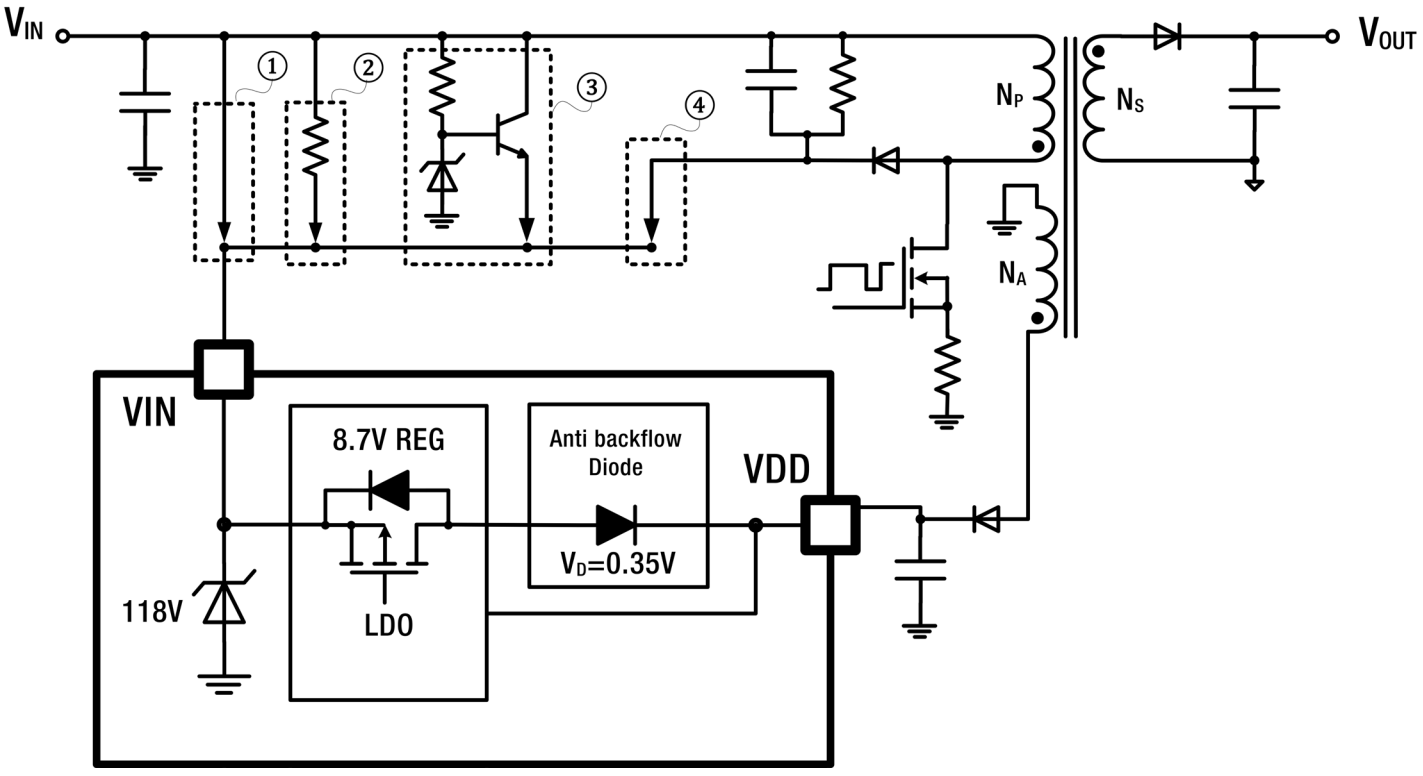


Fig. 20

Typical Application

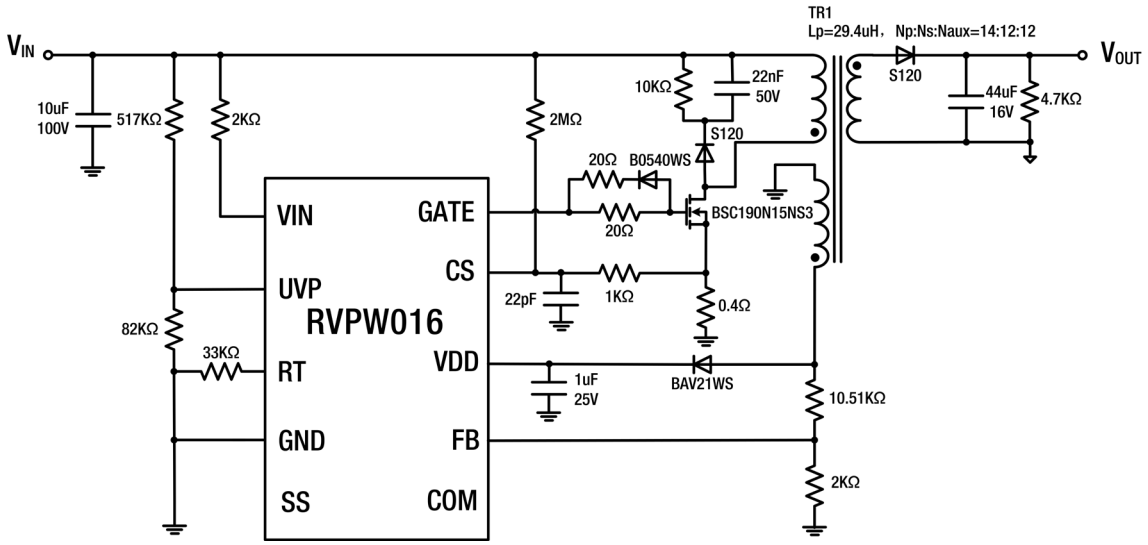


Fig. 21

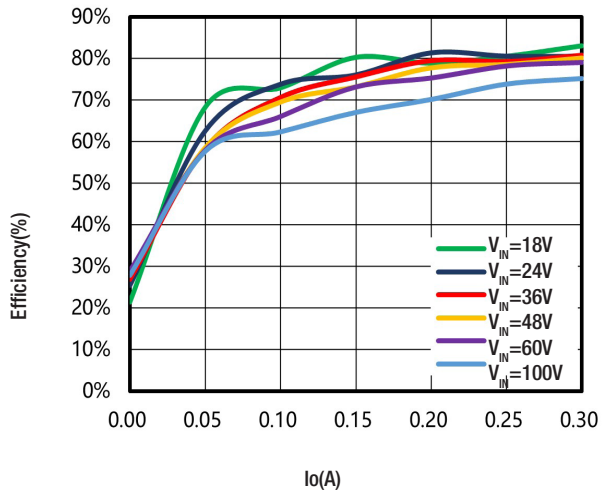


Fig. 22 Efficiency vs Io

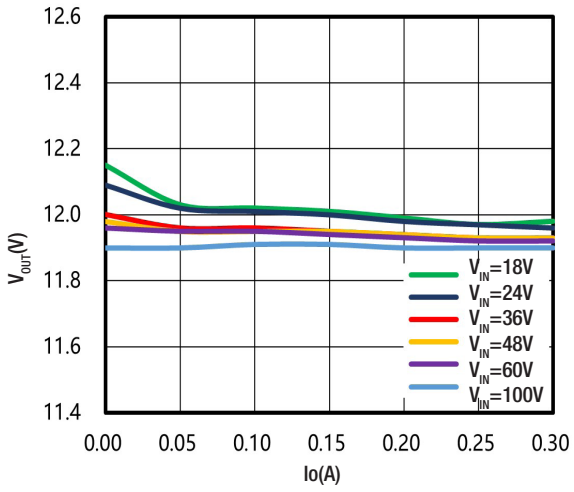
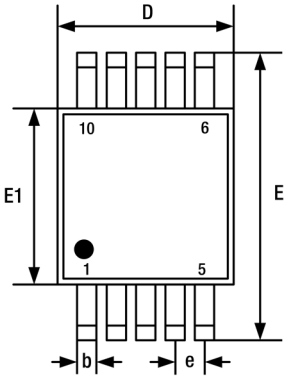


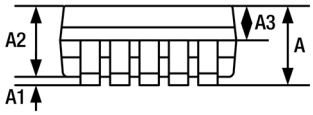
Fig. 23 Vout vs Io

PACKAGING INFORMATION

MSOP10

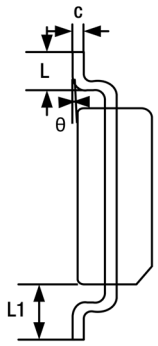


Package top view

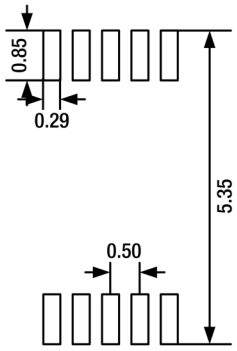


Package front view

DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	---	---	1.10
A1	0.05	---	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	---	0.26
c	0.15	---	0.19
D	2.900	3.000	3.100
E	4.70	4.90	5.10
E1	2.900	3.000	3.100
e	0.50 BSC		
L1	0.95 REF		
L	0.40	---	0.70
θ	0°	---	8°



Package side view



Recommended solder pads

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVPW016-FJH-R	MSOP10	10	Tape and Reel	5000	RVPW016	MSL-3

*Marking Code :
RVPW016—— Product Code