Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDA5V0B20P1Q0 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

ESD protection device in an ultra-small DFN0603 Surface-Mounted Device (SMD) plastic package designed to protect two automotive In-vehicle network bus lines from the damage caused by Electrostatics discharge (ESD) and other transients.

The TESDA5V0B20P1Q0 may be used to provide ESD protection up to ±30kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 5A (8/20μs) according to IEC61000-4-5.

FEATURES

- AEC-Q101 qualified
- ESD protect for 1 line with bidirectional
- Provide ESD protection to

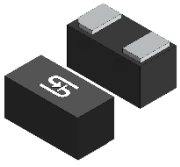
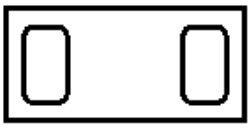
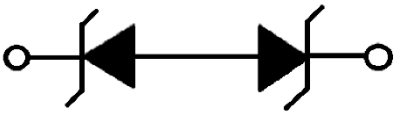
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV(contact)

  IEC 61000-4-4 (EFT) 40A (5/50ns)

  IEC 61000-4-5 (Lightning) 5A (8/20us)
- Suitable for 5V and below, operating voltage applications
- Ultra small packages save board space
- Protect one I/O line or one power line
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

APPLICATION

- Portable medical devices
- Smart phones
- PDAs

PACKAGE: DFN0603-2L	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Typical peak pulse power (tp = 8/20us)	P_{PK}	56	W
Peak pulse current (tp = 8/20us)	I_{PP}	5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Operating junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	-	8.2	-	V
Reverse leakage current	V_{RWM} = 5V, T_J = 25°C	I_R	-	3.7	500	nA
Clamping voltage(1)	I_{PP} = 1A, tp = 8/20us	V_C	-	9.0	-	V
	I_{PP} = 2A, tp = 8/20us		-	9.5	-	V
	I_{PP} = 5A, tp = 8/20us		-	11.2	-	V
Clamping voltage(2)	I_{TLP} = 4A, tp = 100ns	V_{CL}	-	10.3	-	V
	I_{TLP} = 16A, tp = 100ns		-	15.6	-	V
Junction capacitance	1MHz, V_R = 0V	C_J	-	16.5	20	pF
	1MHz, V_R = 2.5V		-	12.4	-	pF
Dynamic resistance(2)		R_{DYN}	-	0.44	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TESDA5V0B20P1Q0 M6G	DFN0603-2L	15,000 / 7" Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

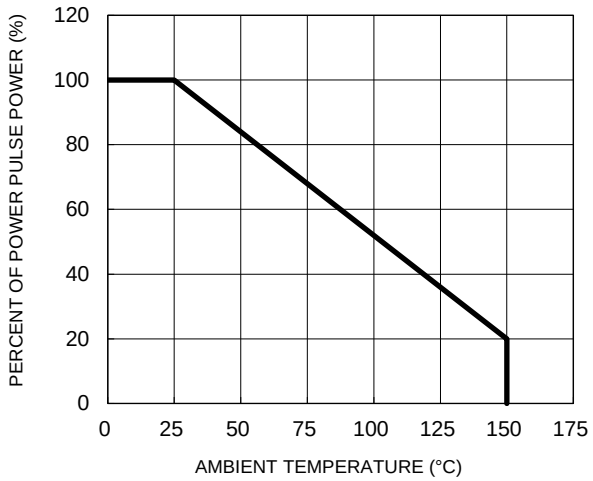


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

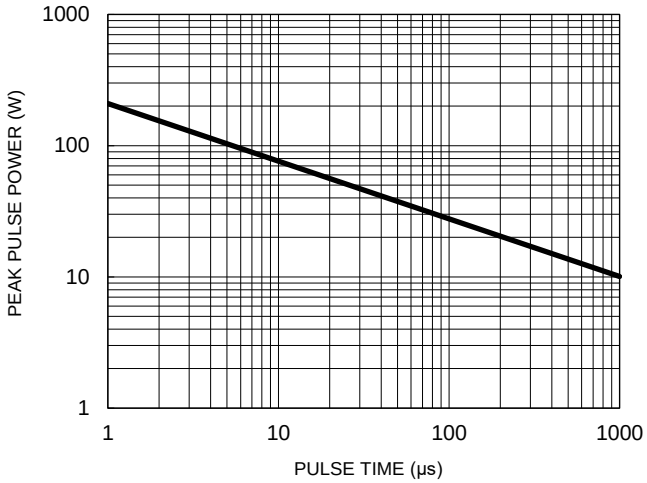


Fig.3 Clamping Voltage vs. Peak Pulse Current

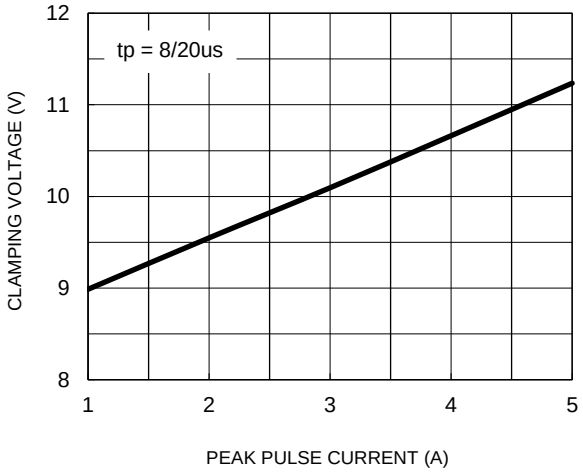


Fig.4 Capacitance vs. Reverse Voltage

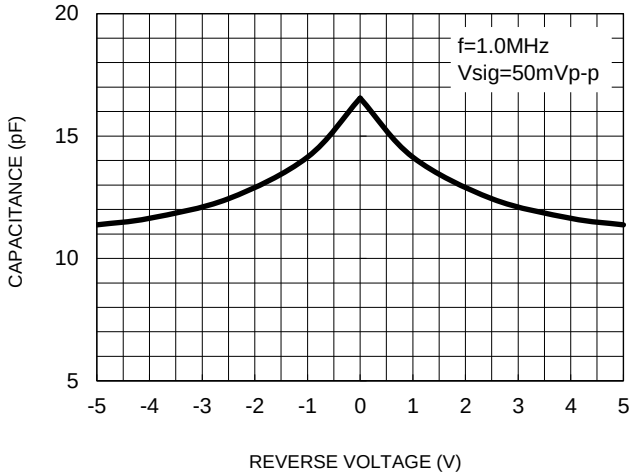
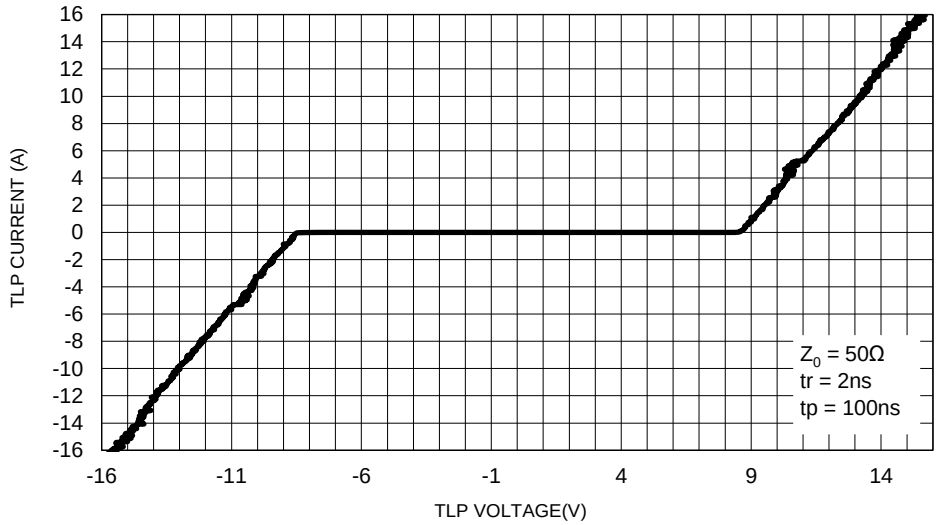


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform per IEC61000-4-5

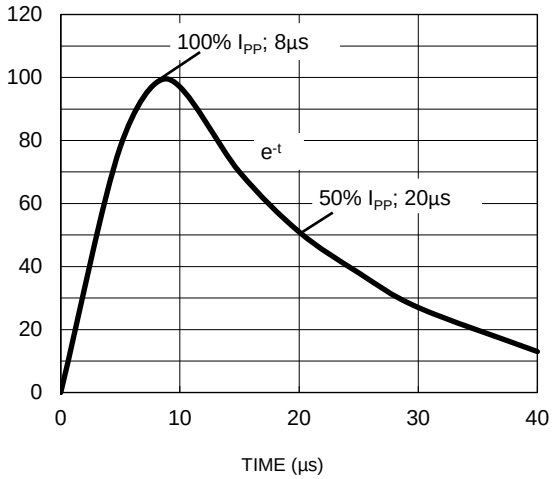
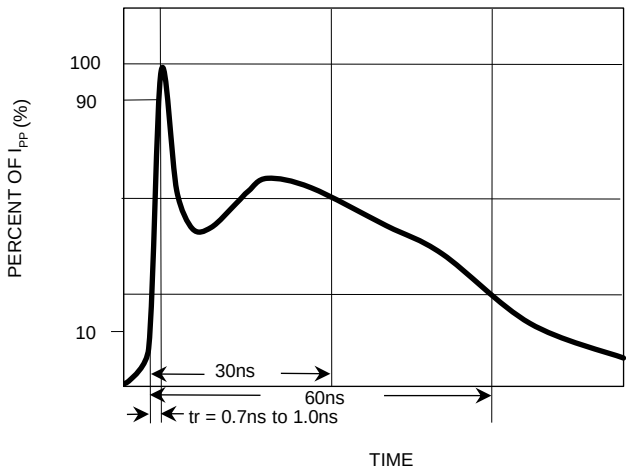


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

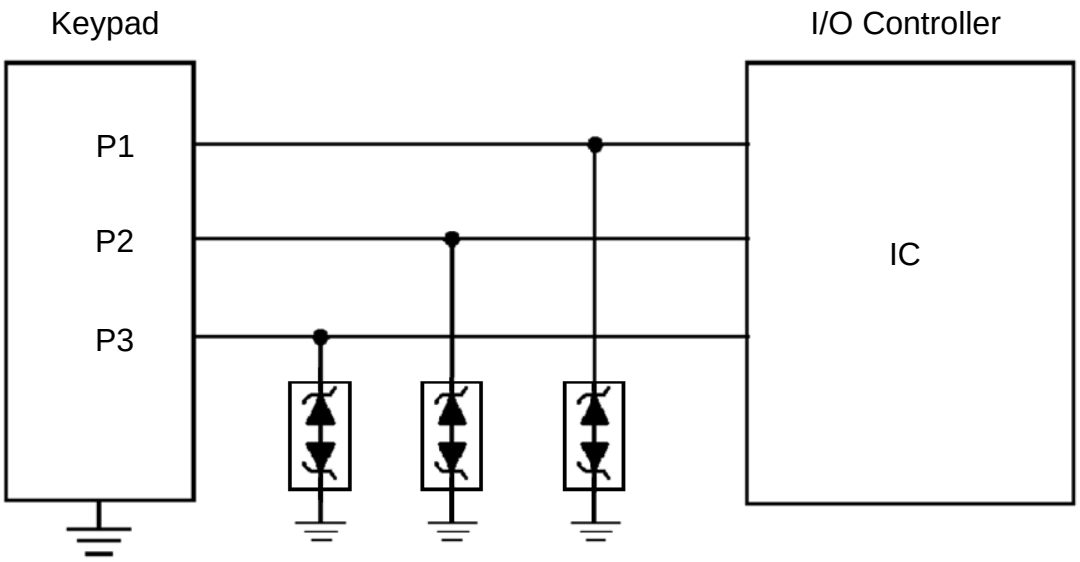
Device Connection

The TESDA5V0B20P1Q0 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.
The usage of the TESDA5V0B20P1Q0 is shown in Fig1.Protected line.
To minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDA5V0B20P1Q0 should be kept as short as possible.

To obtain enough suppression of ESD transient, a good circuit board is critical. Thus, the following guidelines are recommended:

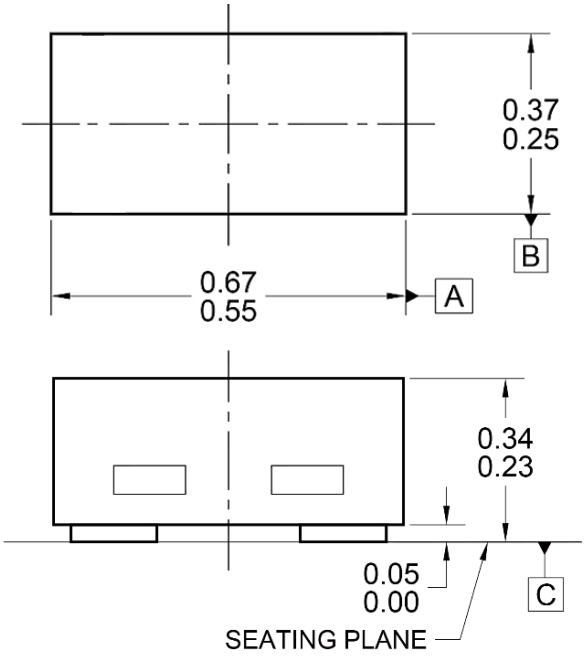
- Let the path length between the protected lines and the TESDA5V0B20P1Q0 minimize.
- Place the TESDA5V0B20P1Q0 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground plane whenever possible.

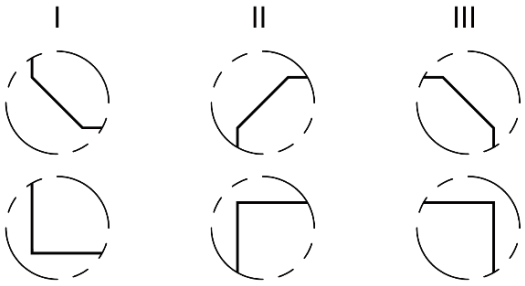
Fig.1 ESD protection by TESDA5V0B20P1Q0



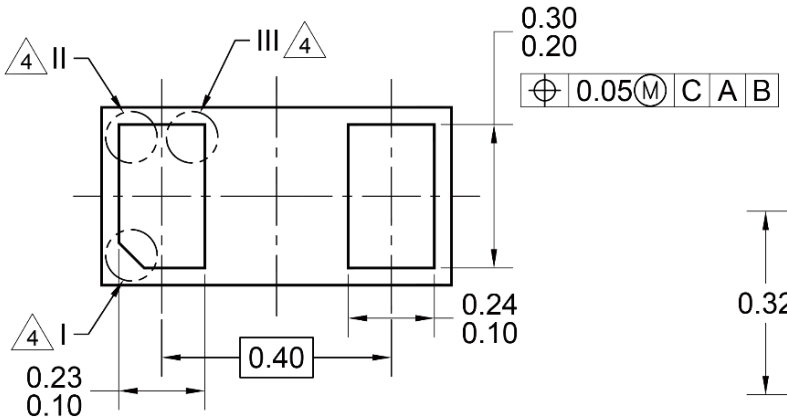
PACKAGE OUTLINE DIMENSIONS

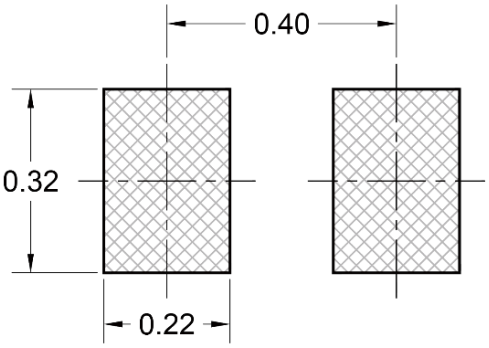
DFN0603-2L





CATHODE TERMINAL
CORNER NOTCH OPTION





SUGGESTED PAD
LAYOUT

MARKING DIAGRAM

CE = Device Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE SIZE CODE REFERENCE:
   EIA (inch) NAME: 0201 (0.024in x 0.012in)
   IEC (metric) NAME: 0603 (0.6mm x0.3mm)

4 CATHODE TERMINAL MAY HAVE CHAMFER NOTCH OR FULL 90 DEGREES CORNER.

5. DWG NO. REF: HQ2SD07-DFN0603-067 REV C.

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